THERMAL CHARACTERIZATION ABSTRACTION FOR INTEGRATED OPTOELECTRONICS

by

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ABSTRACT

Advances in *silicon photonics* are enabling hybrid integration of optoelectronic circuits alongside current complementary metal-oxide-semiconductor (CMOS) technologies. To fully exploit the capability of this integration, it is important to explore the effects of thermal gradients on optoelectronic devices. The sensitivity of optical components to temperature variation gives rise to design issues in silicon on insulator (SOI) optoelectronic technology. The thermo-electric effect becomes problematic with the integration of hybrid optoelectronic systems, where heat is generated from electrical components. Through the thermo-optic effect, the optical signals are in turn affected and compensation is necessary. To improve the capability of optical SOI designs, optical-wave-simulation models and the characteristic thermal operating environment need to be integrated to ensure proper operation.

In order to exploit the potential for compensation by virtue of resynthesis, temperature characterization on a system level is required. Thermal characterization within the flow of physical design automation tools for hybrid optoelectronic technology enables device resynthesis and validation at a system level. Additionally, thermally-aware routing and placement would be possible. A simplified abstraction will help in the active design process, within the contemporary computer-aided design (CAD) flow when designing optoelectronic features.

This thesis investigates an abstraction model to characterize the effect of a temperature gradient on optoelectronic circuit operation. To make the approach scalable, reduced order computations are desired that effectively model the effect of temperature on an optoelectronic layout; this is achieved using an electrical analogy to heat flow. Given an optoelectronic circuit, using a thermal resistance network to abstract thermal flow, we compute the temperature distribution throughout the layout. Subsequently, we show how this thermal distribution across the optoelectronic system layout can be integrated within optoelectronic device- and system-level analysis tools.

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CHAPTER 1

INTRODUCTION

Recent breakthroughs in silicon-based integrated optics – dubbed *silicon photonics* – are establishing the viability of large-scale, on-chip integration of nano-photonic devices with electronic circuits. Such developments include, for example, demonstration of high-speed silicon optical modulators [1, 2], silicon continuous wave lasers [3], hybrid silicon-compatible fabrication methods for lasers [4], their use in optical links [5], among many others [6, 7]. The semiconductor industry finds these developments particularly encouraging; *Si*-photonics offer the potential for low-latency, low-power, and high-bandwidth interconnect solutions for on-chip communications fabric [8–11]. Hybrid integration of optical circuits with electronic chips is enabling applications far beyond traditional roles of optics in communications – such as *optical digital logic* [12, 13], *quantum and reversible computation* [14–16], *networks-on-chips* [17], *signal sensing and processing* [18], etc. Corporations such as Intel, IBM, and HP are investing heavily in silicon photonics integration for computing systems [19, 20]; also significant are the open foundry initiatives and developmental programs, such as the OPSIS framework [21].

As the availability and applications of integrated optics expand, the need for automated design space exploration, optimization, and physical synthesis of integrated electro-optical systems is also beginning to appear. For this reason, the Electronic Design Automation (EDA) community has recently begun investigations into automatic synthesis techniques (problem models, abstractions, tools, and algorithms) required to fully exploit the potential for optoelectronic integration [10, 22–25]. Our research group at the University of Utah is also investigating design automation techniques for logic and physical synthesis of integrated optics [12, 26–29]. As a part of the effort, *this thesis investigates* an abstraction technique to characterize the effect of (externally generated) temperature gradients on the operation of optoelectronic systems.

1.1 Motivating Scenario

Dense on-chip integration of electronic and optical circuits poses the problem of thermal-aware design and synthesis of integrated optics. In dense, high-performance Very-Large-Scale Integration (VLSI) applications, high-frequency switching of a large number of transistors causes large amounts of power to be dissipated on-chip. This leads to elevated temperatures (hot-spots) on the VLSI chip, and the resulting temperature gradient can cause timing failures, a reduction in the lifetime of the chip, and even cause material stresses that may result in cracking of the chip [30].

Considering a three-dimensional chip stacking topology, a photonic layer is integrated over an existing electronic design such as multi- or many core processors and cache memory (Fig. 1.1). In this case, the optical layer can be designed by way of an optical network-on-chip (ONoC) interconnecting these processors together for parallel processing (Fig. 1.2). The underlying computational units, or cores, will generate heat resulting in scheduled core switching. The generated temperature gradient may cause undesired thermo-optic effects — particularly thermal modulation of the refractive index of the material — causing the optical layer to function incorrectly.

In the VLSI domain, temperature-aware physical design automation has received a lot of attention [30–33]. The floorplanning, placement, and routing of VLSI modules is further

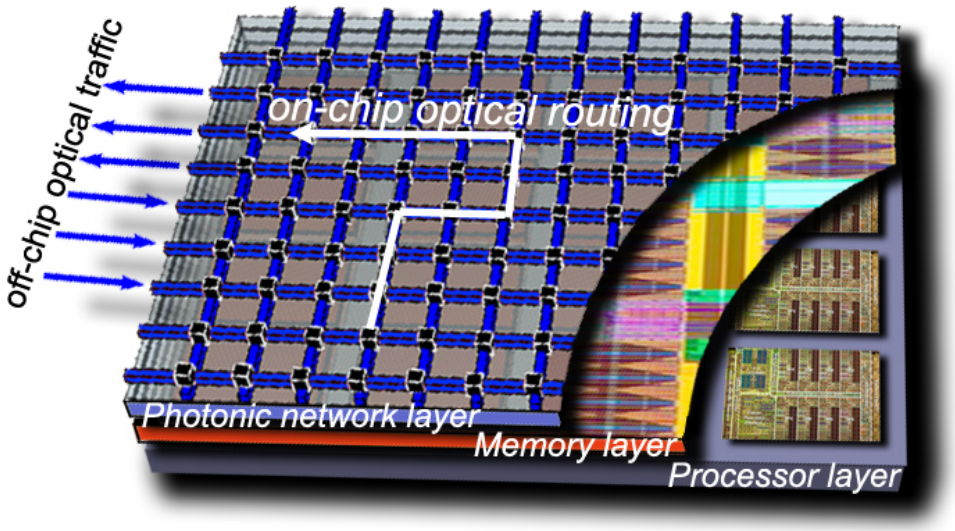


Figure 1.1: Artistic rendition of a hybrid optoelectronic processor that uses a photonic interconnect for global routing.

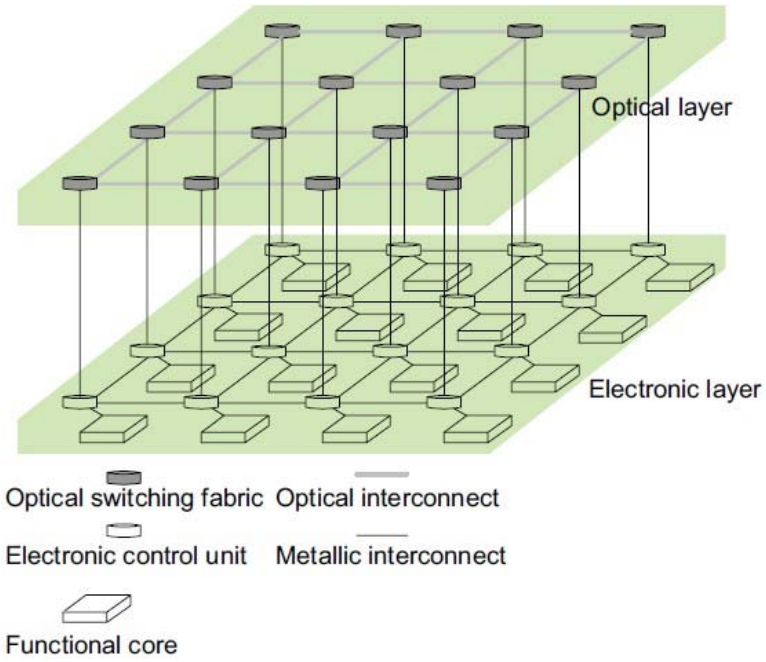


Figure 1.2: Optical routing in multicore application

augmented by interpolating thermal constraints, thereby generating a layout that will mostly "even out" the thermal profile. Thermal analysis and thermal-aware design is also an important part of the integrated optics design space [34, 35]. However, contemporary techniques are applicable mostly to the discrete design of optical components, and they do not scale to larger systems.

At a system level, it is desirable to *develop thermal models* (abstractions) that can be used to characterize the effect of *external* temperature gradients on optical layout operation. Such abstractions will be an essential component of synthesis tools for i) floorplanning, placement, and routing for optical systems under external temperature gradients; and ii) postplacement thermal-aware compensation techniques, at the system-level [17].

1.2 Problem Statement

Given a layout of an optoelectronic circuit, we assume that the circuits consist of ring resonators, Mach-Zehnder interferometers, splitters, couplers, and waveguides where modulation is caused by free-carrier injection by employing a PIN junction surrounding the waveguide (ring). Also given an external thermal gradient as a set of discrete temperature

sources T_i that are placed at arbitrary locations (x_i, y_i) below the optical layout will be provided. We want to compute the resulting gradient as it spreads through a photonic layer. Knowing the temperature, we wish to determine (or estimate) optoelectronic device functionality in the thermally effected regions.

Once determined, the impacted device's functionality can be minimized through passive compensation. This is achieved by transforming the temperature gradient into an average temperature within the device(s) of interest. Subsequently, this information will be converted into a change in the refractive index (Δn). These changes in refractive index will be related to changes in the phase of the signal, the operating bandwidth, and other metrics such as quality factor (Q) of the resonator, free-spectral-range (FSR) of the resonator, etc. The novelty of this technique lies in the abstraction of thermal gradients and their reduced computational model.

Performing full-scale, coupled, 3-D, electromagnetic, and heat transfer simulations for every design, "thermal closure" is computationally infeasible for traditional CAD flow. A reduced order computation will allow the active implementation in CAD flow integrated development environments (IDEs) – Synopsys, Cadence, Mentor Graphics, etc.

It is important to *contrast the need for thermal-abstraction in optical systems against the need for high-resolution thermal modeling* in VLSI chips. In VLSI, transistor performance and metal conductivity are both temperature dependent. Given the high layout density, on-chip VLSI thermal modeling must achieve nanometer resolutions [30]. On the other hand, an optical chip layout is not as dense. Additionally, the device size is an order of magnitude larger than CMOS gates — 90 - 150 nm waveguide thickness and 10 μm ring diameters are typical device sizes in contemporary optical device libraries. Therefore, the thermal effect modeling and characterization problems can be made scalable by deriving approximation models – *abstractions* – without compromising system-level performance estimates.

Analysis is performed to determine the order complexity in the reduced model as compared to full-simulations. Order of discretization is analyzed as a feasibility study. Work has been performed to *validate* the abstraction model by comparing to full-scale simulations. Validation is important here, because abstraction models should reduce order complexity; however, they must remain accurate.

This thesis is organized as follows: Chapter 2 covers previous work and explains the

novelty of the research. Chapter 3 describes the technical background necessary for a general understanding of heat transfer, refractive index, optical field propagation in waveguides, optical devices, the finite difference method, and the Alternating Direction Implicit (ADI) tridiagonal matrix algorithm for solving these types of problems. Chapter 4 covers the research involved in creating the proposed abstraction model, an implementation of this model on an optical layout, and a generalized algorithm. Additionally, Chapter 4 covers the validity of the model as compared to full-scale simulation and discusses our results. Chapter 5 details how we can use this abstraction model in device-level synthesis. Chapter 6 describes future research plans related to this work and concludes this thesis.

CHAPTER 2

LITERATURE REVIEW

The main focus of the investigation presented in this thesis is geared toward *architectural* exploration for photonic interconnection networks in multicore processor systems [8–10, 17, 23, 25]. At the functional/logic-design level, there have been investigations into the use of optical components as building-blocks, connected by waveguides, to design optical computing systems [12, 26, 36, 37]. Specialized computing applications such as *quantum and reversible computing* in the optical domain are also being investigated [14, 16]. High-level synthesis, using technology-mapping, provided with a library of optical device building-blocks has also been presented [22]. The focus of these works is on *architectural and functional analysis and optimization*; physical design and fabrication details are beyond the scope of such works.

At the much lower (physical) level, [24] demonstrates a *full-custom layout* of photonic structures using a commercial CMOS-based layout editor (Cadence Design Systems Virtuoso). Waveguide curves are discretized at a fine level into rectangular geometry, enabling waveguides to be represented in a format that traditional foundries accept. This methodology is significant in that it provides a building-block pathway for producing foundry-ready layouts and masks for non-Manhattan device geometries (i.e. rings, arcs, waveguide curvature). However, "design automation" is essentially absent, and the design must be conceived of and optimized manually. Similarly, most of the commercially available Photonics CAD suites (i.e. RSoft [38], Lumerical [39], etc.) provide a framework for physical device design, analysis, and finite-difference time-domain (FDTD) simulation engines for performance analysis of optical design components. However, automated techniques for design space exploration during physical synthesis – *automated floorplanning, placement, waveguide routing* while optimizing for physical parameters such as thermal effects, insertion-loss, bend-loss, phase coherence issues, etc. – are not available.

The inherent capability to estimate thermal gradients and the incorporation of their impact as a design constraint has not been explored for optical design. Integration of these design constraints is necessary to provide reliable system integration. However, incorporating these thermal-aware design constraints into the contemporary CAD flow may require integration at multiple levels of design.

2.1 Challenges in CMOS Nanophotonics

Silicon is the mainstay of the semiconductor industry. The ease of manufacturing for semiconductors in well-characterized silicon-based processes, and steady improvements in performance and density at each process node, makes CMOS-based technology the dominant computing manufacturing technology. For the same reasons, attempts are also made to develop silicon-based integrated optics – *silicon photonics* – for hybrid integration.

Researchers from both industry and academia are studying the application of integrated optics into CMOS-based manufacturing for a way to combat the scaling limitations of *Moore's Law* [40]. One problematic aspect of hybrid integration [41] is the sensitivity of the index-of-refraction to temperature variations in the primary CMOS optical guiding material – *silicon*. As we know, integrated electronics are often designed around their thermal constraints [42] to "even out" thermal densities over the area of a chip.

The promise of monolithic integration of photonic networks in silicon-based processes opens the door to a great number of opportunities in system design. Optics, once an exclusively telecom technology, is now able to leverage advanced processes in fabrication and integration [43]. This change enables far greater flexibility and complexity in design, and the ability for designers to investigate novel methods for utilizing optics in systems.

Investigations have been made into optical digital signal processing [44], sensing, and even computing frameworks that can leverage optics in ways that would have been cost-prohibitive. In essence, we are now seeing a *convergence of computation and communications.* Already a number of architectures have been proposed for connecting systems via optical interconnect networks [9, 45], including as separate layers in 3D topologies [46–50]. However, when hybrid integration occurs, electrically generated gradients are what can be problematic in these proposed multilayered 3D topologies.

What is lacking is an overall infrastructure incorporating temperature as a *design con-*

straint in the CAD flow of system integration using advanced methodologies. Advanced methodologies exist for the characterization of electrical systems based on internal heat generation due to high-powered and fast-switching devices [51]. However, these methods do not provide the flexibility to model any variations on these problems. Generally, modeling heat diffusion from an external gradient is of interest. Furthermore, we want to know how heat diffuses through the multiple layers in a optoelectronic layout – this problem has not manifested itself as a focal point until now.

2.2 Thermal Analysis of Optical Systems

At the device level, analysis of thermal effects on waveguides [34, 35] has been studied and acknowledges that temperature can dramatically effect the optical performance of interferometric devices such as Mach-Zehnder interferometers and ring resonators in terms of power, absorption, and phase. Athermal and/or thermally-tuned design of modulators [52, 53] is well studied in literature. [52] proposed an athermal micro-ring resonator that can operate at 22 ± 1 C. [53] claims to demonstrate interoperability of devices over a wide temperature range of 80 degrees. However, these topics have not been explored fully at the system level – particularly, their integration into design flow.

The work of [17] takes a step in this direction; however, it proposes an operating system-level thermal-aware scheduling algorithm for managing traffic though an optical-NoC. Robust scheduling algorithms are indeed remarkable; however, they are not only increasing power consumption but would be compensating at a steady-state. Reduced-order steady-state thermal modeling and passive compensation techniques are not a subject of these works but may prove useful when used together with techniques such as [17].

Textbooks, such as [54], acknowledge the fact that temperature is a modulating factor of optical devices. However, they do not acknowledge that external gradients will introduce strain on device- and system-level performance. Other textbooks, such as [55], do acknowledge this fact, but still the topics have not been fully explored at a system design level.

2.3 Routing and Placement in VLSI

Computation of thermal gradients on VLSI chips, with nanometer scale resolution, has been addressed by the EDA community [56, 57]. These techniques are generally based on finite-element, finite-difference, and Green function-based methods. Thermal-aware synthesis techniques make use of these algorithms for module placement [30, 33, 58], routing [32], and also for thermal-via placement [59] for heat dissipation in VLSI chips.

Force-directed placement has been explored in electronic VLSI [33, 58]. Here thermal forces are incorporated into the objective function of quadratic programming-based optimization. This may prove to be a useful formulation for the placement using thermal forces of optical devices. Non-Force-Directed methods have been implemented as well [30]. A Non-Force-Directed method incorporates temperature into a Simulated Annealing algorithm which may also be useful in the optical domain.

Routing and placement algorithms for optical devices and networks have been explored in contemporary literature [25, 60]. GLOW [25], a stand-alone router, incorporates a local temperature variation profile as a constraint in a channel assignment problem using integer linear programming. However, there is no mention of how to compute a thermal variation profile nor does it change depending on the routing. PROTON [60], an automatic place-and-route tool specific to optical NoCs, implements a quadratic program to estimate waveguide crossings using probability estimation. Once placed, a modified Lee's Algorithm is used for the routing with predefined penalty factors allowing waveguide crossings when necessary.

The problem that we address is somewhat different than the ones addressed in the above works. We wish to derive an *abstraction model* to estimate the effect of an *external thermal gradient* on the operation of an optical layout. To the best of our knowledge, this particular problem has not been addressed before and is therefore investigated in this thesis.

CHAPTER 3

PRELIMINARY CONCEPTS

This chapter covers the fundamental concepts involved in optical device designs, governing functions of optical wave propagation and properties of dielectric materials, heat-diffusion, and the finite-difference method and the ADI tridiagonal matrix algorithm. These theories will be described in enough detail to guide the reader through the material required for a general understanding of the characteristics of optical signals.

3.1 Optics, Optical Devices, and Properties

Transmitting optical beams through dielectric conduits is known as guided-wave optics. Initially developed to provide long-distance light transmission without the necessity of using relay lenses, this technology has matured to the level of integration using the standard CMOS processes of fabrication. Integrated optics is the technology of combining, on a single substrate ("chip"), various optical devices and components useful for generating, focusing, splitting, combining, isolating, polarizing, coupling, switching, modulating, and detecting light [61]. Optical waveguides, or interconnects, provide the links among these components. Integrated optics has miniaturized optics in much the same way that integrated circuits have served to miniaturize electronics.

3.1.1 Interconnects

The mechanism for guiding light in photonic waveguides is total internal reflection (TIR). TIR is the phenomenon where light is completely reflected at a dielectric interface without the help of reflective coatings. The key requirement for TIR is that the light must be incident on a dielectric interface from a high index of refraction side. Thus an optical waveguide must consist of a layer of high index of refraction dielectric surrounded by material with a lower index of refraction.

Fig. 3.1 shows three commonly used typed of waveguides. A traveling ray within the

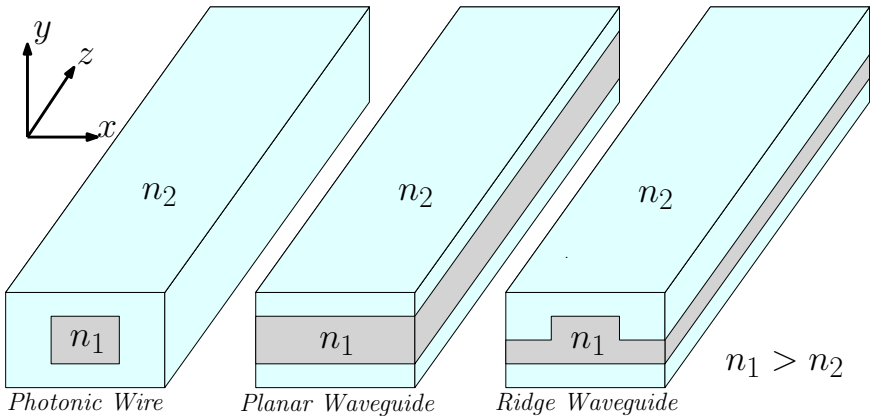


Figure 3.1: Three commonly used waveguide geometries

high index material will be totally-internally-reflected at the upper and lower interfaces of a waveguide structure if the angle of incidence at the interface exceeds the critical angle. However, the essential idea behind the optical waveguide is that light is trapped in a high index media through TIR, but changes to the refractive index will alter the behavior of the light (Eqn. (3.27)).

3.1.2 Wave Optics

Silicon photonics concepts are not very different from the electromagnetics used in electronics. Information still travels by means of waves and is governed by variations of the electromagnetic wave equation.

Consider the symmetric planar waveguide shown in Fig. 3.1. Maxwell's equations can be written in terms of the refractive index $n_{i=1,2}$ of the three layers and by assuming that the material of each layer is nonmagnetic and isotropic, i.e. $\mu = \mu_0$ and ϵ is a scalar, we have:

$$\nabla \times \mathbf{E} = -\mu_0 \frac{\partial \mathbf{H}}{\partial t} \quad (3.1)$$

$$\nabla \times \mathbf{H} = n_i^2 \epsilon_0 \frac{\partial \mathbf{E}}{\partial t} \quad (3.2)$$

$$\nabla \cdot \mathbf{E} = 0 \quad (3.3)$$

$$\nabla \cdot \mathbf{H} = 0 \quad (3.4)$$

To obtain the above equations from the generalized Maxwell's equations, the following substitutions were made:

$$\mathbf{D} = \epsilon \mathbf{E} = n^2 \epsilon_o \mathbf{E} \quad (3.5)$$

$$\mathbf{B} = \mu_o \mathbf{H} \quad (3.6)$$

$$\mathbf{J} = 0 \quad (3.7)$$

$$\rho = 0 \quad (3.8)$$

If we apply the curl operator to Eqn. (3.1), we get:

$$\nabla \times \nabla \times \mathbf{E} \quad = \quad -\mu_o n_i^2 \epsilon_o \frac{\partial^2 \mathbf{E}}{\partial t^2} \tag{3.9}$$

where Eqn. (3.2) has been used to eliminate **H**. To simplify further we can use the following vector identity.

$$\nabla \times \nabla \times \mathbf{A} \quad = \quad \nabla \cdot (\nabla \cdot \mathbf{A}) - \nabla^2 \mathbf{A} \tag{3.10}$$

where **A** is an arbitrary vector field. Using Eqn. (3.3) and (3.10), Eqn. (3.9) an be simplified to:

$$\nabla^2 \mathbf{E} \quad = \quad \mu_o n_i^2 \epsilon_0 \frac{\partial^2 \mathbf{E}}{\partial t^2} \tag{3.11}$$

Writing the above equation in phasor notation (assuming a time-harmonic field of the form $e^{-j\omega t}$), we obtain:

$$\nabla^2 \mathbf{E} \quad + \quad k_o^2 n_i^2 \mathbf{E} = 0 \tag{3.12}$$

which is the three-dimensional vector wave equation for a uniform dielectric with refractive index n_i. Here k_o is the free-space wave number given by:

$$k_o \quad = \quad \omega \sqrt{\mu_o \epsilon_o} \tag{3.13}$$

The electric field vector **E** in Eqn. (3.13) is a phasor quantity, which is complex and has both a magnitude and a phase. In addition, **E** is in general a function of space coordinates x, y, z and angular frequency ω. **E** is independent of time since the time dependence has been removed by the phasor transformation.

We may simplify Eqn. (3.12) by assuming that the structure is uniform in the y-direction (Fig. 3.1) and extends to infinity in the y-direction. This allows us to assume that the field **E** is also uniform in this direction. Thus $\frac{\partial}{\partial y}$ is replaced by zero. If we further assume a z dependence of the form $e^{j\beta z}$, with β as the longitudinal propagation constant, Eqn. (3.12) is simplified and takes the form:

$$\frac{d^2 \mathbf{E}}{dx^2} + (k_o^2 n_i^2 - \beta^2)\mathbf{E} = 0 \tag{3.14}$$

The above equation is known as the *Helmholtz Equation*. In this case, **E** is a function of x only and the equation is a second order ordinary differential equation. The propagation constant β can be expressed as:

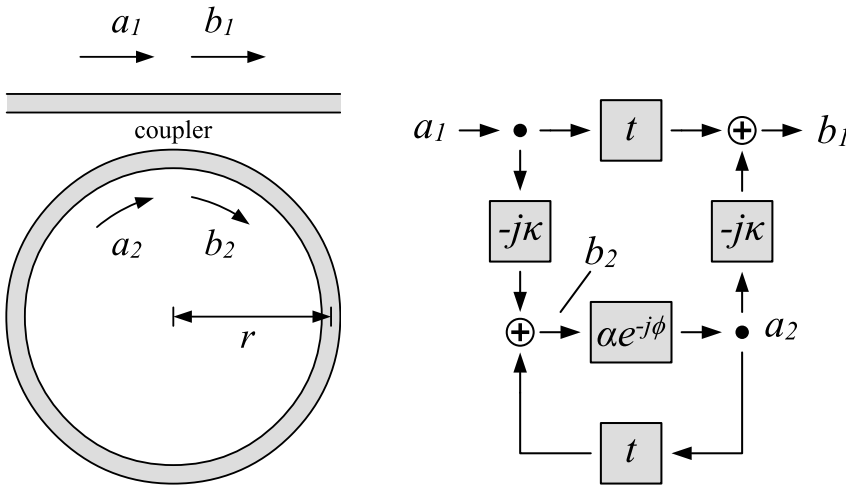
$$\beta = k_o n_{eff} \tag{3.15}$$

where n_{eff} is called the effective index. The field of a planar waveguide is in general a superposition of Transverse Electric (TE) polarized field and Transverse Magnetic (TM) polarized field. The field components of the two polarizations are H_x, E_y, and H_z for TE-polarized waves and E_x, H_y, and E_z for TM-polarized waves.

3.1.3 Ring Resonators

Optical ring resonators are wavelength filtering devices with a notch-filter-type response curve centered around a resonant wavelength. These devices rely on a resonance condition, which causes light within the ring to destructively interfere with light on the coupling waveguides. Alternatively, with two straight waveguides coupled to a single ring, a ring resonator can be used to couple specific wavelengths into or out of a waveguide in a 2x2-switch type operation. Consider the ring resonator structure depicted in Fig. 3.2a, where a ring of radius r is coupled to a straight waveguide. The coupler is assumed to be symmetrical, and also lossless, implying that the coupling coefficient K is related to the transmission coefficient t by: $K^2 + t^2 = 1$. The ring has an overall length of $L = 2\pi r$, and round-trip loss coefficient α.

A functional model (block diagram) for the ring resonator structure is depicted in 3.2b. The electric field amplitude E_{b_2} is the sum of the input electric field E_{a_1} coupled into the ring with coefficient K, and the round-trip feedback of the ring E_{a_2} coupled back into the ring with coefficient t. Likewise, E_{b_1} is the sum of the t-coupled input signal E_{a_1} and the



(a) Ring resonator (b) Block diagram

Figure 3.2: Structure of an optical ring resonator

K-coupled signal E_{a_2}. These are expressed as:

$$E_{b_2} = \frac{-jKE_{a_1}}{1 - t\alpha e^{-j\phi}} \tag{3.16}$$

$$E_{a_2} = E_{b_2}\alpha e^{-j\phi} \tag{3.17}$$

$$E_{b_1} = tE_{a_1} - jKE_{a_2} \tag{3.18}$$

where $\phi = \beta L$ is the phase produced by the round-trip traversal of the ring from b_2 to a_2. The $-j$ factor attached to K is the result of coupling from one waveguide to another: the latter signal always lags the former by a 90° phase shift.

Combining Eqn. (3.18) and squaring the result to determine power, results in:

$$\frac{P_{b_1}}{P_{a_1}} = \left|\frac{E_{b_1}}{E_{a_1}}\right|^2 = \frac{\alpha^2 + |t|^2 - 2\alpha|t|\cos\phi}{1 + \alpha^2|t|^2 - 2\alpha|t|\cos\phi} \tag{3.19}$$

The value of Eqn. (3.19) drops to zero (0) when two conditions are met:

1. critical coupling, and

2. the resonance condition

The *resonance condition* that constrains the round trip of the ring is defined as:

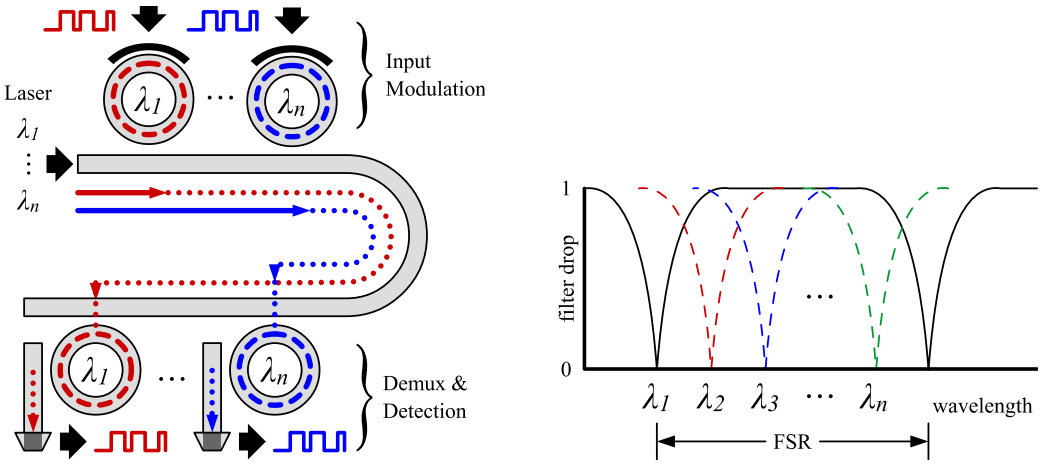
$$\phi = \beta L = 2\pi m \tag{3.20}$$

where m is an integer. The dependence of ϕ on β implies that resonance is wavelength and waveguide (i.e. effective index) dependent and a useful relationship is derived:

$$\beta L = \frac{2\pi n_{eff}}{\lambda_0} L = 2\pi m \quad \rightarrow \quad n_{eff} L = m\lambda_0 \tag{3.21}$$

where n_{eff} is the effective index of the waveguide and λ_0 is the freespace wavelength of light.

Ring resonators also have a free spectral range (FSR), the $\Delta\lambda$ between resonance peaks depicted in Fig. 3.3b. More formally, the FSR is defined as: FSR $= \frac{\lambda_0^2}{n_g L}$ where n_g is the dispersion-dependent *group index* of the waveguide: $n_g = n_{eff} - \lambda\frac{\partial n_{eff}}{\partial\lambda}$. For more details, the reader is referred to [62].



(a) Modulation and demultiplexing/detection

(b) Channel wavelengths within the FSR of a WDM ring-resonator

Figure 3.3: Function of an optical ring resonator

3.2 Steady-State Heat Conduction

The heat transfer equation can be derived from the general form of heat diffusion (Eqn. (3.22)) to formulate the relationship between change in refractive index and temperature of the medium. The general form of the heat diffusion equation is represented as:

$$\frac{\partial T}{\partial t} = \alpha_T \nabla^2 T \tag{3.22}$$

where α_T is the thermal diffusivity and T is the temperature at a given point.

Now to apply the variables of the materials that will be used to represent the thermal diffusivity coefficient, this can be done using the following equation:

$$\alpha_T = \frac{k}{C_p \rho} \tag{3.23}$$

where C_p is the heat capacity at constant pressure, ρ is the density of the material, and k is the thermal conductivity of material.

Substituting Eqn. (3.23), back into Eqn. (3.22), results in the heat transfer equation of a closed system:

$$C_p \rho \frac{\partial T}{\partial t} - k \nabla^2 T = 0 \tag{3.24}$$

Eqn. (3.24) represents a system with no sources or absorption (sink) of heat. Over time, this system will find equilibrium (i.e. exhibit distributive cooling). Once a heat source or sink is added, the equation becomes (assuming the thermal conductivity is isotropic):

$$C_p \rho \frac{\partial T}{\partial t} - k \nabla^2 T = Q \tag{3.25}$$

where Q is a heat source or sink.

3.2.1 Thermal Dependency

Now to take this one step further, there is a relationship between temperature and refractive index as shown below in Eqn. (3.26).

$$n = n_0 - \alpha(T) \cdot (300K - T) \tag{3.26}$$

where $\alpha(T)$ is the thermo-optic coefficient as a function of temperature, $\alpha_{\text{Si}} \approx 1.86 \times 10^{-4}$, and $0.62 \times 10^{-5} \leq \alpha_{\text{SiO}_2} \leq 1.28 \times 10^{-5}$.

As we can see, there is a clear relationship between the heat transfer equation, Eqn. (3.25), and the dependence of refractive index on temperature. The optical electromagnetic wave equation, Eqn. (3.14) shows the nature of refractive index dependence on signal propagation. Now, the three equations discussed, Eqns. (3.25), (3.26), and (3.14), are all coupled together forming a complex system for any numerical solver in electromagnetics to handle.

As a thermal gradient is distributed through a material, the refractive index directly changes, producing a transient effect on signal propagation [63]. The transient effect can be described as:

$$\Delta\phi = \frac{2\pi}{\lambda}\Delta n_{eff} L_h = \frac{2\pi}{\lambda} L_h \frac{\partial n_{eff}}{\partial T}\Delta T \tag{3.27}$$

where $\Delta\phi$ is the phase shift induced, λ is the wavelength of light, Δn_{eff} is the change in the effective refractive index, L_h is the length of region exposed to heat, and ΔT is the change in temperature.

A major challenge to on-chip ring-resonator integration is their extreme sensitivity to refractive index changes [62]. *Process and geometric variations, and also thermal effects, can shift a ring's resonance off its designed wavelength.* Silicon-based ring-resonators are especially susceptible to temperature-induced changes in refractive index (n) due to silicon's large thermo-optic coefficient of $dn/dT = 1.86 \times 10^{-4}/^{\circ}K$. Resonance shifts of $0.1nm/^{\circ}K$ have been reported, causing high bit-error-rates (BERs) for a δT of a few degrees [64]. In systems such as those depicted in Fig. 1.1, thermal gradients pose significant operational challenges. Fig. 3.4 depicts what a thermal gradient would look like if it were present under an optical design. We can see that a temperature around some of the rings can penetrate into the ring structure and potentially deem the ring(s) inoperable.

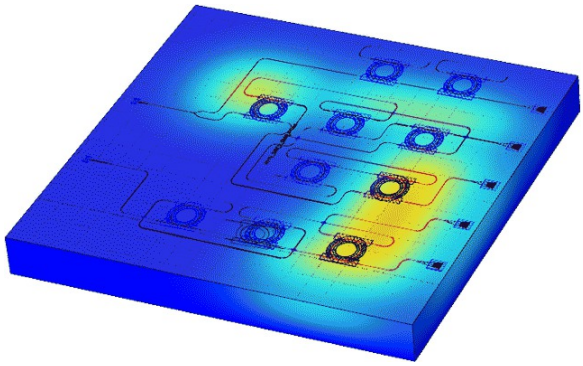


Figure 3.4: On-chip heat sources creating thermal gradients across an optical substrate

3.3 Thermal Gradient Computation

There are many situations where obtaining an exact solution of a partial differential equation (PDE) is not possible and we have to resort to approximations in which the infinite set of values in the continuous solution is represented by a finite set of values referred to as the *discrete* solution.

Modeling these *discrete* processes is based on a variety of numerical methods among which finite difference method (FDM) and finite element method (FEM) are the most popular. It is often believed that FEM is superior compared to other methods since it can accurately follow material interfaces. This is widely used in engineering when deformation of complex isolated objects is modeled. However, in general there are particular advantages of using FEM. This is mainly related to the necessity of capturing large deformations of complex viscous, elastomer, and/or plastic materials with strong lateral variations of physical properties and to the absence of constant predefined material interfaces.

In contrast to FEMs that are quite complex to study and implement, FDMs are both simple and powerful. They offer possibilities to model a wide range of complex natural processes with numerical approaches that are easy to understand and implement in computer programming. We seek both making rapid progress and obtaining strong numerical modeling background – therefore, FDM is a better choice. So for the implementation of our abstraction model, we have chosen to use an FDM to implement our nondynamic system of constant predefined material interfaces, boundaries, and coefficients.

3.3.1 Finite Difference Method

The idea of solving differential ordered problems with analytical solutions is limited to highly simplified problems in simple geometries. A better way to model these problems is to exploit the idea that an ”approximate” solution is usually more accurate that the ”exact” solution of a crude mathematics problem. This is the result of the degree of difficulty to formulate the problem exactly as it is. The numerical methods for solving differential equations are based on replacing the differential equations by algebraic equations.

The principle of finite difference methods is close to the numerical schemes used to solve ordinary differential equations. It consists of approximating the differential operator by replacing the derivatives in the equation using differential quotients. The domain is partitioned in space and in time and approximations of the solution are computed at the space or time points. The error between the numerical solution and the exact solution is determined by the error that is committed by going from a differential operator to a difference operator. This error is known as the *discretization error* or *truncation error*. The term truncation error reflects the fact that a finite part of a Taylor series is used in the approximation [65].

For the sake of simplicity, we shall consider the one-dimensional case only. The main concept behind any finite difference scheme is related to the definition of the derivative of a smooth function u at a point $x \in \mathbb{R}$:

$$u'(x) = \lim_{h \to 0} \frac{u(x+h) - u(x)}{h}$$

and to the fact that when h tends to 0 (without vanishing), the quotient on the right-hand side provides a ”good” approximation of the derivative. In other words, h should be sufficiently small to get a good approximation. It remains to indicate what exactly is a good approximation, in what sense. Actually, the approximation is good when the error committed in this approximation (i.e. when replacing the derivative by the differential quotient) tends toward zero when h tends to zero. If the function u is sufficiently smooth in the neighborhood of x, it is possible to quantify this error using a Taylor expansion.

3.3.2 Numerical Formulation

Conduction problems can be solved by finite-difference approximations to the differential equations. An equation is formulated for each node and the set of equations solved

for the temperatures throughout the body. In formulating the equations, we can use a resistance concept, discussed further in Chapter 4, for writing the heat transfer between nodes. Designating our node of interest with the subscript i and the adjoining nodes with subscript j, we have the general-conduction-node situation as shown in Fig. 3.5.

At steady state, the net heat input to node i must be zero or

$$q_i + \sum_j \frac{T_j - T_i}{R_{ij}} = 0 \tag{3.28}$$

where q_i is the *heat flux* delivered to node i by heat generation, radiation, etc. *Heat flux* or *thermal flux* is the rate of heat energy transfer through a given surface and is measured in W/m^2. The thermal resistance (R_{ij}) can take the form of convection boundaries, internal conduction, etc., and Eqn. (3.28) can be set equal to some residual for a relaxation solution or to zero for treatment with matrix and iterative methods.

Although no new information is conveyed by using a resistance formulation, designers may find it convenient to think in these terms. When a numerical computation is to be performed that takes into account property variations, the resistance formulation is particularly useful. Additionally, there are many heat-transfer problems where it is convenient to think of convection and radiation boundary conditions in terms of the thermal resistance they impose on the system [66]. In non-steady-state problems the term thermal impedance is employed as a synonym for thermal resistance but incorporating a dynamic time response. Most importantly, the thermal resistance formulation is also useful for numerical solution of complicated three-dimensional shapes.

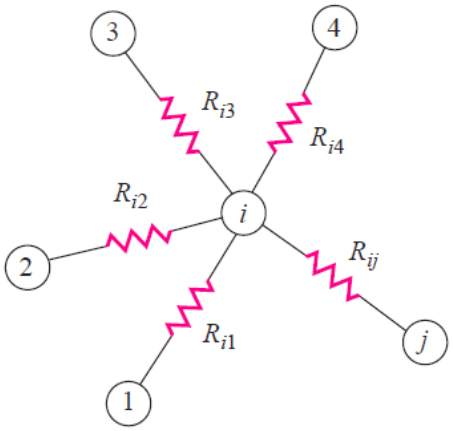


Figure 3.5: General conduction node

The 7-point finite-difference discretization (Fig. 3.6) of Eqn. (3.25) can be obtained through application of the backwards Euler formula which results in an interior point formula,

$$\begin{aligned}\frac{T_{i,j,k}^{n+1} - T_{i,j,k}^{n}}{\Delta t} = \\ &\frac{T_{i+1,j,k}^{n+1} + T_{i-1,j,k}^{n+1}}{R_x} + \\ &\frac{T_{i,j+1,k}^{n+1} + T_{i,j-1,k}^{n+1}}{R_y} + \\ &\frac{T_{i,j,k+1}^{n+1} + T_{i,j,k-1}^{n+1}}{R_z} - \\ &2 \cdot T_{i,j,k}^{n+1} \left(\frac{1}{R_x} + \frac{1}{R_y} + \frac{1}{R_z} \right) + Q_{grad}\end{aligned} \tag{3.29}$$

where Δt, Δx, Δy, and Δz are discretized steps in temporal and spatial dimensions, respectively. R_x, R_y, and R_z are defined as

$$R_x = \frac{\Delta x}{k \Delta y \Delta z}, R_y = \frac{\Delta y}{k \Delta x \Delta z}, \text{ and } R_z = \frac{\Delta z}{k \Delta x \Delta y} \tag{3.30}$$

For steady-state analysis, the term on the left in Eqn. (3.29) can be dropped, resulting in a linear algebra problem as can be solved by the ADI Tridiagonal Matrix Algorithm.

3.3.3 Alternating Direction Implicit Tridiagonal Matrix Algorithm

The Alternating Direction Implicit (ADI) method is a finite difference method for solving partial differential equations. The ADI method is an example of an *operator splitting* method which allows the unwieldy decomposition of PDE's into simpler subproblems and treat them individually (i.e. *separable* problems).

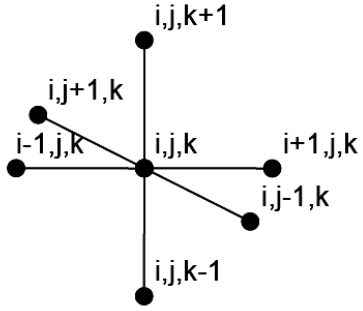


Figure 3.6: 7-point finite-difference stencil

The form of the PDE to be studied is:

$$f = au_{xx} + au_{yy} + au_{zz} + su, \quad (x, y, z) \in \Omega \tag{3.31}$$

where $\Omega \in \mathbb{R}^3$ is bounded on all sides. We will also assuming mixed (Robin) boundary conditions are applied on all of $\partial\Omega$, although we observe that the theory can be developed for other typical boundary conditions. Also note that a, s, and f may all be functions of (x, y, z).

When we discretize Eqn. (3.31) with backward difference approximations, the resulting system of linear algebraic equations take the form

$$Au = b \tag{3.32}$$

Thus, A has the structure of a discrete Laplacian as seen in Fig. 3.7a. In block notation, the matrix has the following structure:

$$A = \begin{pmatrix} A_{xy} & -I & & \\ -I & A_{xy} & -I & \\ & -I & A_{xy} & -I \\ & & -I & A_{xy} \end{pmatrix} \tag{3.33}$$

$$A_{xy} = \begin{pmatrix} A_x & -I & \\ -I & A_x & -I \\ & -I & A_x \end{pmatrix} \tag{3.34}$$

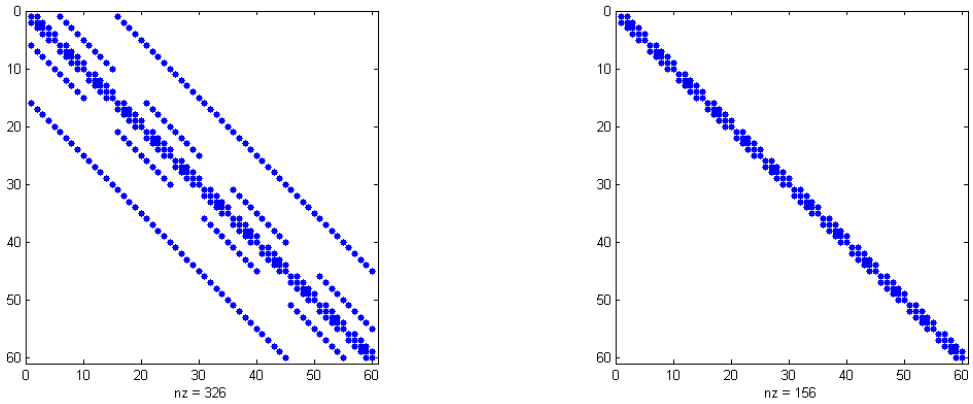
$$A_x = \begin{pmatrix} 6 & -1 & & & & \\ -1 & 6 & -1 & & & \\ & -1 & 6 & -1 & & \\ & & -1 & 6 & -1 & \\ & & & -1 & 6 & -1 \\ & & & & -1 & 6 \end{pmatrix} \tag{3.35}$$

Now we decompose the matrix A as

$$A = H + V + S \tag{3.36}$$

where each of the matrices on the right-hand side is $n \times n$, and each comes from a specific term in Eqn. (3.31). The H, V, and S matrices arise in the discretization of the x, y, and z derivative terms, respectively. From a natural ordering of A in which the vertical index is varied, these matrices have structures depicted in Fig. 3.7.

The tridiagonal structure of these coefficient matrices allows for efficient tridiagonal algorithms that take advantage of the sparse structure. For example, the Tridiagonal Matrix



(a) A matrix

(b) H matrix

(c) V matrix

(d) S matrix

Figure 3.7: FDM coefficient matrix $(5 \times 3 \times 4)$

Algorithm (Thomas Algorithm) is a simplified Gaussian elimination specially formulated for the sparse structure of our coefficient matrix [67]. For such a system, the solution can be obtained in $O(n)$ operations instead of $O(n^3)$ operations as required by a full Gaussian elimination.

CHAPTER 4

MODEL ABSTRACTION

The objective of this thesis, as outlined in Chapter 1.2, is to create a reduced computational model of steady-state heat conduction and apply it to optical structures to characterize their operations. The goal is to define the diffusion of heat through the various regions of media used in the SOI technology for optical devices effectively and efficiently. As mentioned in Section 3.3.2, we will use an electrical analogy to represent, what can be, fairly complicated structures.

4.1 Electrical Analogy

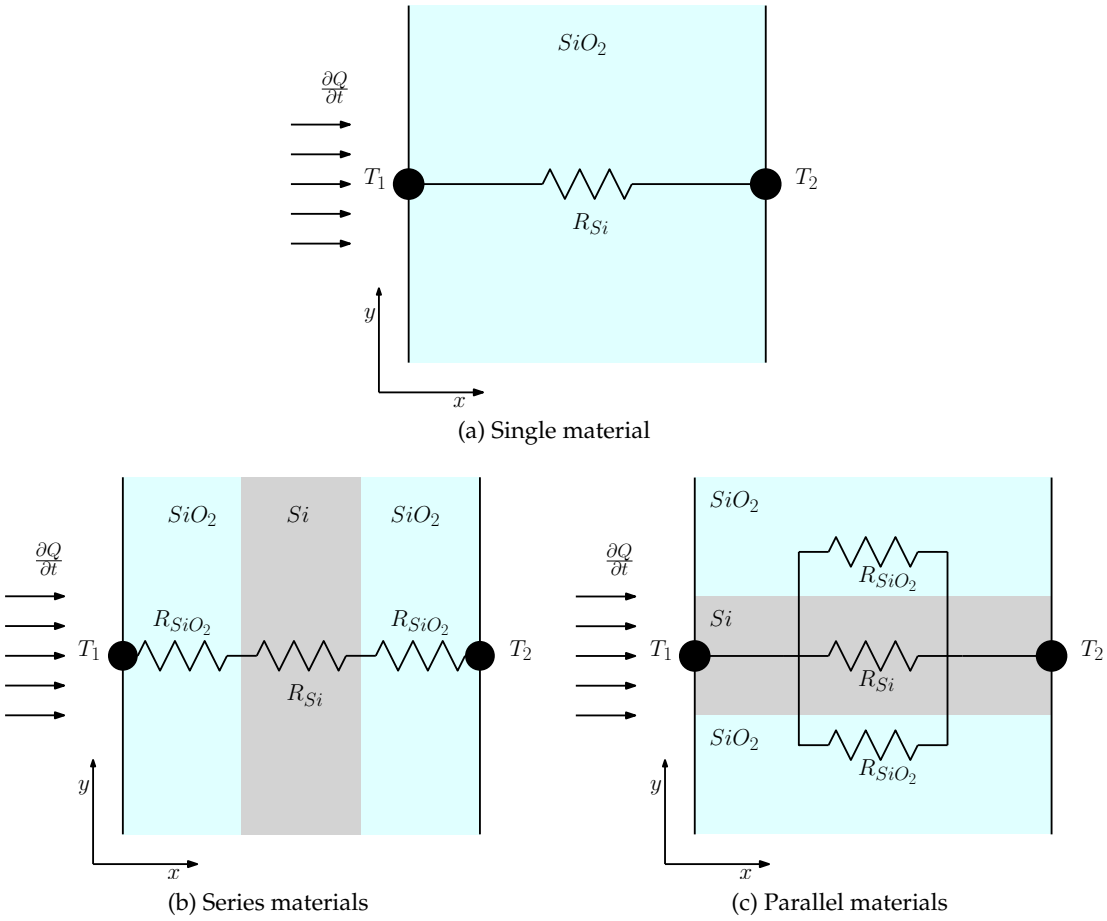
Using an electrical analog to heat conduction [68], we exploit the planar geometry of the problem enabling us to reduce a full detailed 3-D model to *lumped elemental layers* with similar structure.

4.1.1 Analysis in One Dimension

The analog of current I is heat flux q, and potential difference becomes temperature difference between two points $T_1 - T_2$ as illustrated in Fig. 4.1a. This allows us to define a term for the thermal resistivity as follows:

$$R_{thermal} = \frac{L}{A \cdot k_{material}} \tag{4.1}$$

where $R_{thermal}$ is the thermal resistance, L is the distance of thermal flow, A is the cross-sectional area, and $k_{material}$ is the thermal conductivity of the material being modeled. For Si the value of thermal conductivity used is $k_{Si} = 149\ W/(m\ K)$ [69], and for SiO_2 the value of thermal conductivity used is $k_{SiO_2} = 1.4\ W/(m\ K)$ [70]. From this perspective, the slab of SiO_2 in Fig. 4.1a is represented purely as a resistance to heat conduction and we can describe it as a linear representation in one dimension similar to that of the node voltage method used elementary circuit theory:



(a) Single material

(b) Series materials

(c) Parallel materials

Figure 4.1: 1D thermal resistance examples

$$q = \frac{T_1 - T_2}{R_{thermal}} \tag{4.2}$$

where q is the *heat flux* which is analogous to electric current. The concept of a thermal resistance circuit allows ready analysis of heat flux. However, as geometries more closely resemble the planar geometry we are likely to see, it becomes more intuitive.

The concept of a thermal resistance circuit allows ready analysis of problems such as the layered medium problem (Figs. 4.1b and 4.1c). In the slabs shown in Fig. 4.1b, the heat flux is constant with x. The resistances are in series and sum to $R = R_{SiO_2} + R_{Si} + R_{SiO_2}$. With T_1 and T_2 as in the previous example, the heat transfer rate (flux) is given by:

$$q = \frac{T_1 - T_2}{R_{SiO_2} + R_{Si} + R_{SiO_2}} \tag{4.3}$$

Another example is a multilayered medium with horizontal stacking (Fig. 4.1c). In this case, the heat transfer resistances are in parallel. Fig. 4.1c shows the physical configuration,

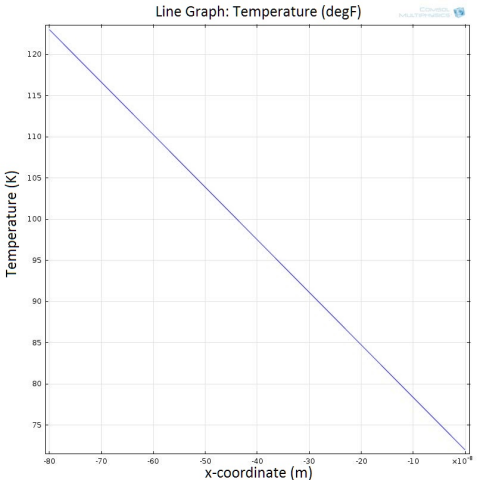
the heat transfer paths, and the thermal resistance circuit. For this situation, the total heat flux consists of the heat flow in the three parallel paths:

$$q = \frac{T_1 - T_2}{R_{SiO_2} \parallel R_{Si} \parallel R_{SiO_2}} \tag{4.4}$$

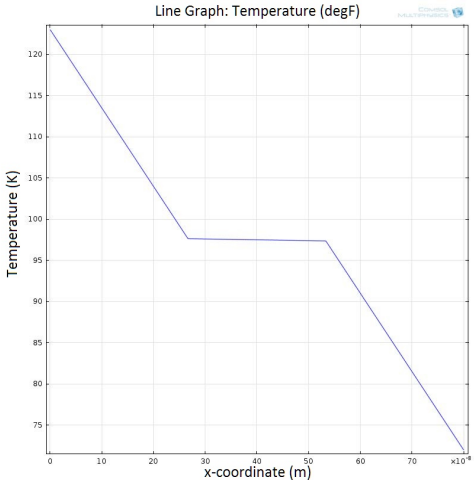
where $\parallel$ is the parallel resistance formula defined as $R_{parallel} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$.

A full-scale 1-D simulation results in a temperature vs. distance plot for the aforementioned three types of analog resistance circuits as depicted in Fig. 4.2 for the respective configurations. We confirm the linear behavior as Eqn. (4.2), (4.3), and (4.4) represent.

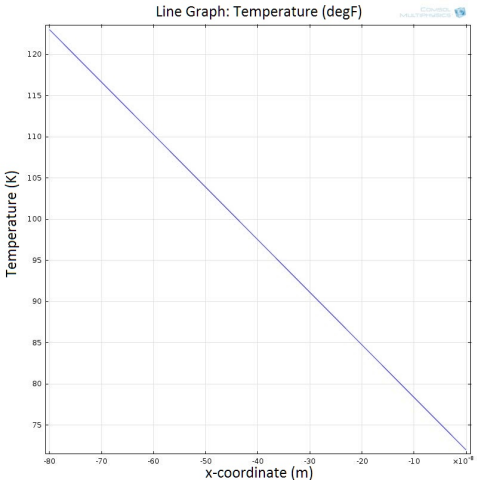
The types of materials and layout geometries we encounter in this investigation are



(a) Single medium



(b) Series media



(c) Parallel media

Figure 4.2: Simulation results (temperature vs. distance) of equivalence thermal resistances

mainly silicon (Si) and silicon dioxide (SiO_2) as illustrated in Fig. 4.3. There are more materials present in contemporary designs; however, this investigation keeps materials to a minimum. We will discuss scalability based on experimental results found in the next chapter.

The experiments performed in one dimension were on a few different configurations. If we look back and see the three examples explored in Fig. 4.1, we see a solid medium and two different cases of stacked media. For the studies performed in one dimension, we show that the thermal resistance analogy produces what you would expect to see from the three different configurations shown in Fig. 4.1. This section was for a general proof of concept and to show that the linear approximations are indeed valid.

Because the nature of an electrical analogy is a linear approximation, we show that the single medium material produces a smooth linear curve 4.2a as Ohm's Law depicts with $V = IR$. And furthermore, the series configuration produces a continuous piece-wise linear representation as one would expect to see from a series of resistors connected together 4.2b. Lastly, the parallel configuration shows again a continuous linear curve but also smooth as one would expect from a parallel combination of resistances – an R_{eq} representation 4.2c. The results described are shown in Fig. 4.2 to confirm the validity of the abstraction in one dimension. Although no implementation was done with one dimension, the experiments were performed in COMSOL to validate the abstraction in one dimension.

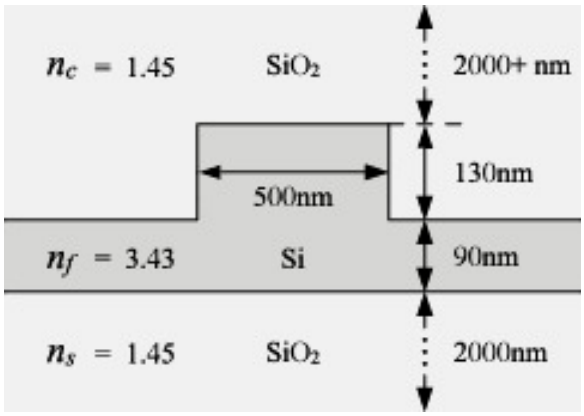
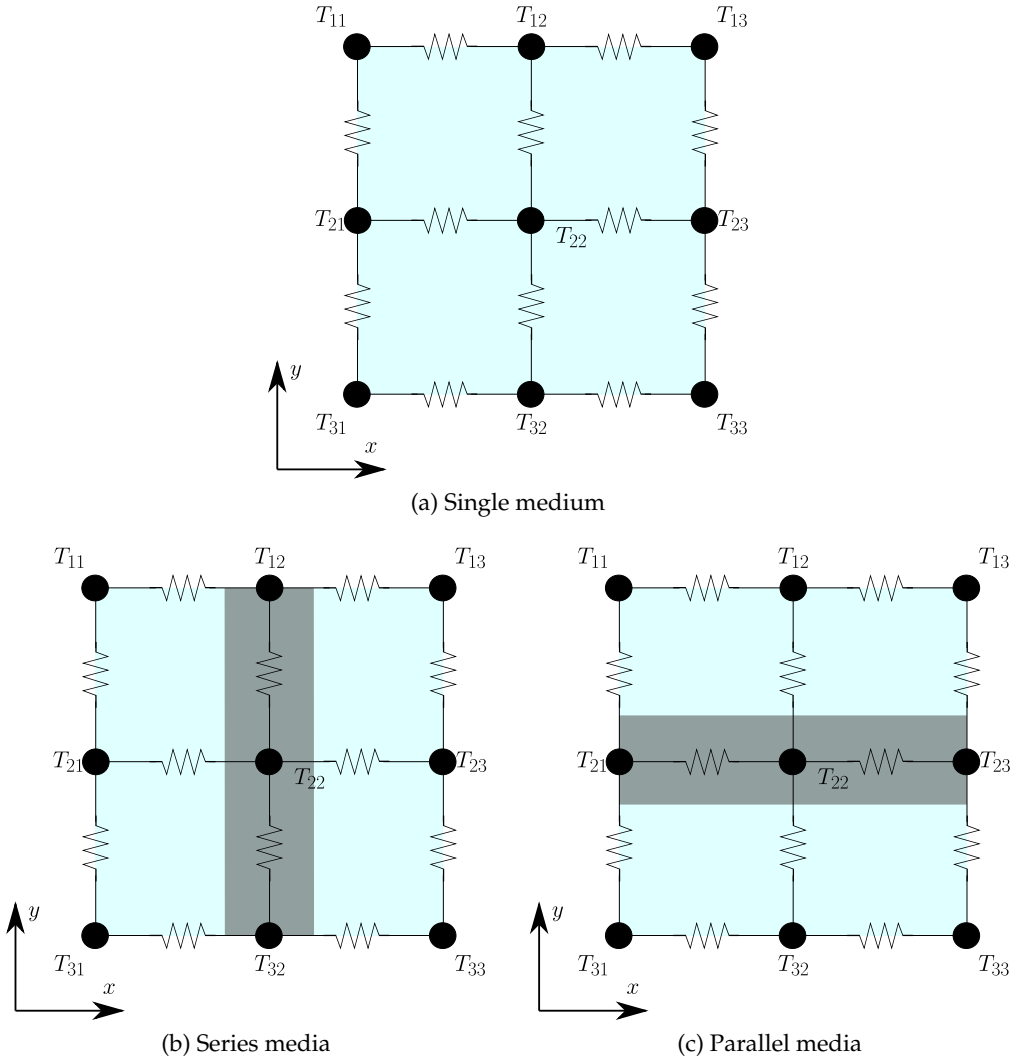


Figure 4.3: Waveguide profile

4.1.2 Analysis in Two Dimensions

As we extend this analogy to a second spatial dimension, heat flow can be analyzed in two dimensions ($\mathbb{R}^2$). We now see that heat flow can be analyzed in the xy plane. In this case, the heat transfer resistances form a network over the entire domain as shown in Fig. 4.4. While this is a linear approximation, such a model abstraction suffices as we are mostly interested in the temperature at the intersections of the lattice structure.

Based on the finite-difference method, we can formulate the steady-state approximation for the interior nodes using the 5-point finite difference discretization. An equation is formulated for each node and solved iteratively for the temperatures throughout the media. Designating our node of interest with the subscript xy and the adjoining nodes



(a) Single medium

(b) Series media

(c) Parallel media

Figure 4.4: 2D thermal resistance examples

with subscript ij where each surrounding node falls into the set $S := \{(x \pm 1, y), (x, y \pm 1)\}$, we have a general-conduction node situation shown in Fig. 3.5. At steady state, the net heat input to node xy must be zero:

$$q_{ij} + \sum_{(i,j) \in S} \left(\frac{T_{ij} - T_{xy}}{R_{ij \to xy}} \right) = 0$$

where q_{ij} is the heat delivered to node ij by heat generation, radiation, etc. The heat we expect to see delivered to certain nodes around the boundaries will be around $80 - 100\ W/cm^2$ as in the Pentium 4 processor [71]. The $R_{ij \to xy}$ can take the form of convection boundaries, internal conduction, etc. To express the overall effect of convection, we use Newton's law of cooling:

$$q = hA(T_{edge} - T_{\infty}) \tag{4.5}$$

Here the heat-transfer rate is related to the overall temperature difference between the domain edge and the medium (possibly air) and the surface area A. The quantity h is called the *convection heat-transfer coefficient* and Eqn. (4.5) is the defining equation. An analytical calculation of h may be made for some systems. However, for more complex situations, it must be determined experimentally. The heat-transfer coefficient is sometimes called the *film conductance* because of its relation to the conduction process between a layer of fluid on a material. From Eqn. (4.5), we note that the units of h are in W/m^2K when the heat flow is in watts.

Typical values to expect for the conditions we see are $h = 5 - 25\ W/(m^2K)$ for free convection of Air and $h = 50 - 150\ W/(m^2K)$ for an optimized heat sink with fans (Fig. 4.5) typically found in a desktop computer [72]. Table 4.1 sums up the relevant nodal represen-

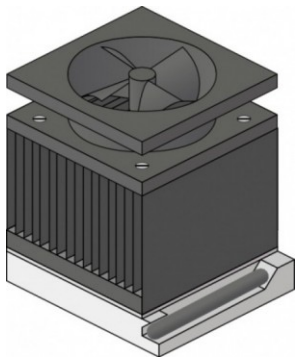
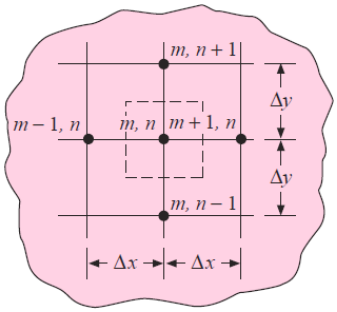
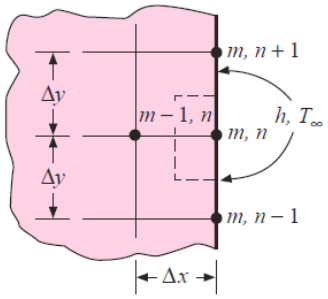
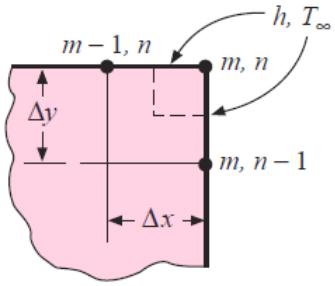


Figure 4.5: Example heat sink

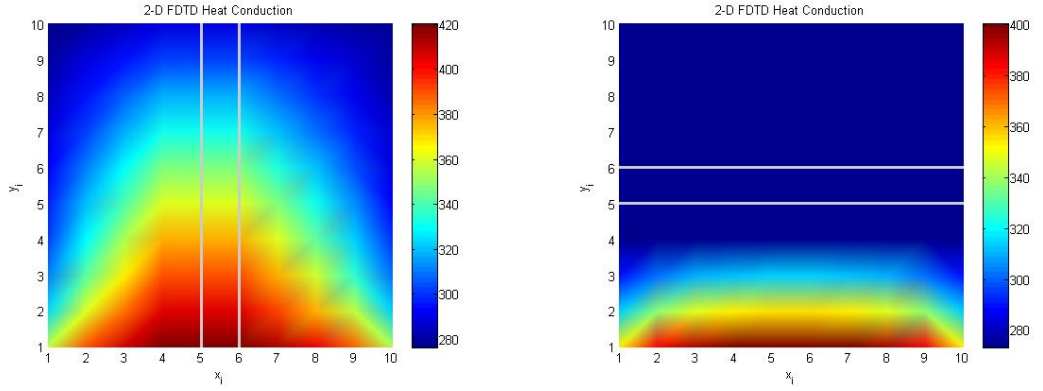
Table 4.1: 2D resistive boundary conditions for illustrated examples

Boundary condition	$\mathbf{R_{m_+}}$	$\mathbf{R_{m_-}}$	$\mathbf{R_{n_+}}$	$\mathbf{R_{n_-}}$
 (a) Interior conduction	$\frac{\Delta x}{k\Delta y\Delta z}$	$\frac{\Delta x}{k\Delta y\Delta z}$	$\frac{\Delta y}{k\Delta x\Delta z}$	$\frac{\Delta y}{k\Delta x\Delta z}$
 (b) Edge convection	$\frac{1}{h_{m_+}\Delta y\Delta z}$	$\frac{\Delta x}{k\Delta y\Delta z}$	$\frac{2\Delta y}{k\Delta x\Delta z}$	$\frac{2\Delta y}{k\Delta x\Delta z}$
 (c) Corner convection	$\frac{2}{h_{m_+}\Delta y\Delta z}$	$\frac{2\Delta x}{k\Delta y\Delta z}$	$\frac{2}{h_{n_+}\Delta x\Delta z}$	$\frac{2\Delta y}{k\Delta x\Delta z}$

tations of resistances and the modifications that are necessary for convection boundaries [66] and illustrations.

Using MATLAB, the 2D-FDM method was implemented and the results can be seen in Fig. 4.6 for series and parallel configurations. The results are as expected – both simulations use the same boundary temperature. *Si* has a higher thermal conductivity then that of SiO_2, creating a path for heat to flow.

In the two-dimensional implementation, a ring resonator was also simulated with a



(a) FDTD - series media (b) FDTD - parallel media

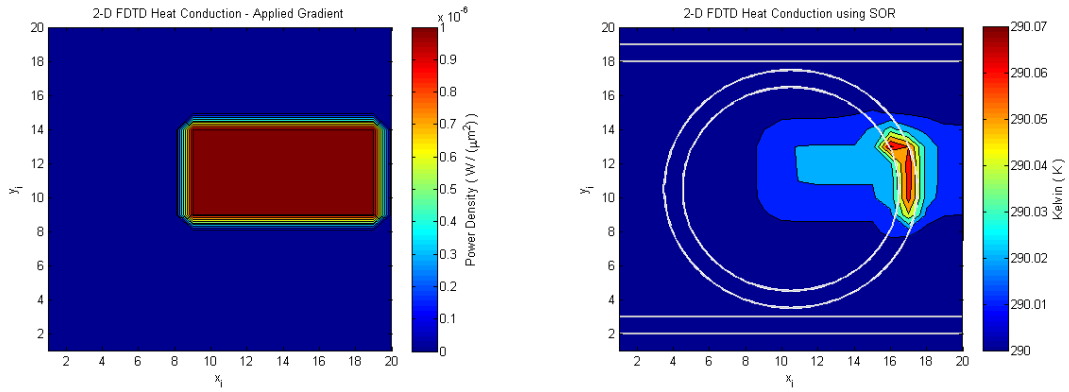
Figure 4.6: Implementation of 2D FDM

footprint of $10\mu m \times 10\mu m$. The results can be seen in Fig. 4.7b. As the behavior of the previous experiment shows, we see the ring conducting more heat due to its Si composition.

4.1.3 Analysis in Three Dimensions

Extending the electrical analogy into the third spatial dimension, heat flow is analyzed in three-dimensional space ($\mathbb{R}^3$). The heat transfer resistances are networked over the entire spatial domain as seen in Fig. 4.8. The connections along the z-axis do have resistors, between nodes, but for visual simplicity they have been omitted. Again, because this is a linear approximation, we are only interested in the temperature at the nodes, as in the one- and two-dimension cases.

This formulation is similar to the two-dimensional expression. However, each node



(a) Applied gradient (b) Simulation result

Figure 4.7: 2D-FDM simulation of ring resonator

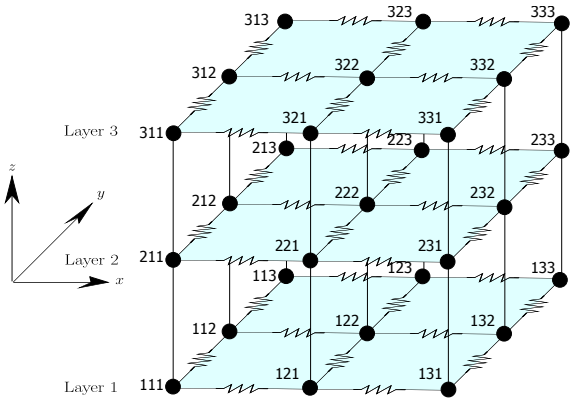


Figure 4.8: 3D thermal resistance example

now has *six neighbors*, a *positive* and a *negative* step for each dimension. The representation for the nodal formulation is as follows:

$$T_{xyz} = \frac{\sum_{(i,j,k)\in \mathbf{S}} \left(q_{ijk} + \frac{T_{ijk}}{R_{xyz\to ijk}} \right)}{\sum_{(i,j,k)\in \mathbf{S}} \left(\frac{1}{R_{xyz\to ijk}} \right)} \tag{4.6}$$

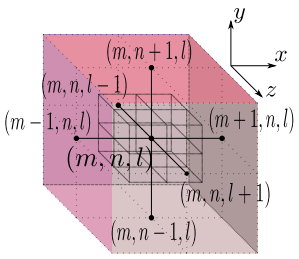
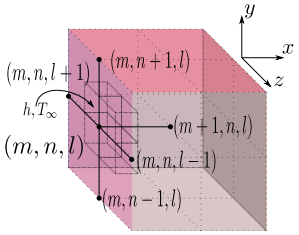
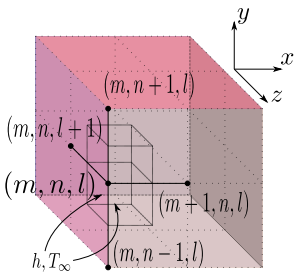
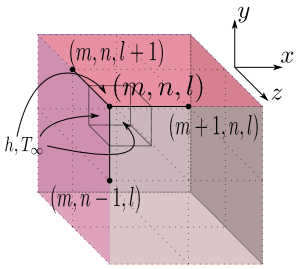
$$\mathbf{S} \in \{(x \pm 1, y, z), (x, y \pm 1, z), (x, y, z \pm 1)\} \tag{4.7}$$

where q_{ijk} is the *heat flux* delivered to node ijk by heat generation, radiation, etc. There are also resistance modifications to account for convection boundary conditions as in the two-dimensional case. These nodal resistances and the modifications necessary for the convection boundary nodes are defined and illustrated in Table 4.2.

Using MATLAB, the 3D-FDM method was implemented to simulate a ring resonator with a footprint of $10\mu m \times 10\mu m$; the results can be seen in Fig. 4.9. This simulation used $h_{air} = 25\ W/m^2K$ as the boundary conditions around the sides to represent free flowing air. We use $h_{sink} = 150\ W/m^2K$ as the condition on the top of the device to represent a heat sink (Fig. 4.5) and rectangular hot-spots with $q_{spot} = 100\ W/cm^2$ representing the typical power density of some modern processors [71].

The outlined region indicates the *Si* ring and waveguides while the other area indicated the SiO_2 cladding. Again, because of *Si*'s higher thermal conductivity than that of SiO_2, the *Si* region conducts heat better than SiO_2 when a source is present under both materials unless well insulated by SiO_2. In Fig 4.9, we can see the heat becomes more concentrated around the *Si* of the waveguide rather than in the surrounding SiO_2 cladding as in previous examples. However, the intensity of heat is different here because we have boundary

Table 4.2: 3D resistive boundary conditions for illustrated examples

Boundary condition	$\mathbf{R_{m_+}}$	$\mathbf{R_{m_-}}$	$\mathbf{R_{n_+}}$	$\mathbf{R_{n_-}}$	$\mathbf{R_{l_+}}$	$\mathbf{R_{l_-}}$
 (a) Interior Conduction	$\frac{\Delta x}{k\Delta y\Delta z}$	$\frac{\Delta x}{k\Delta y\Delta z}$	$\frac{\Delta y}{k\Delta x\Delta z}$	$\frac{\Delta y}{k\Delta x\Delta z}$	$\frac{\Delta z}{k\Delta x\Delta y}$	$\frac{\Delta z}{k\Delta x\Delta y}$
 (b) Face Convection	$\frac{\Delta x}{k\Delta y\Delta z}$	$\frac{1}{h_{m_-}\Delta y\Delta z}$	$\frac{2\Delta y}{k\Delta x\Delta z}$	$\frac{2\Delta y}{k\Delta x\Delta z}$	$\frac{2\Delta z}{k\Delta x\Delta y}$	$\frac{2\Delta z}{k\Delta x\Delta y}$
 (c) Edge Convection	$\frac{2\Delta x}{k\Delta y\Delta z}$	$\frac{2}{h_{m_-}\Delta y\Delta z}$	$\frac{4\Delta y}{k\Delta x\Delta z}$	$\frac{4\Delta y}{k\Delta x\Delta z}$	$\frac{2\Delta z}{k\Delta x\Delta y}$	$\frac{2}{h_{l_-}\Delta x\Delta y}$
 (d) Corner Convection	$\frac{4\Delta x}{k\Delta y\Delta z}$	$\frac{4}{h_{m_-}\Delta y\Delta z}$	$\frac{4}{h_{n_+}\Delta x\Delta z}$	$\frac{4\Delta y}{k\Delta x\Delta z}$	$\frac{4\Delta z}{k\Delta x\Delta y}$	$\frac{4}{h_{l_-}\Delta x\Delta y}$

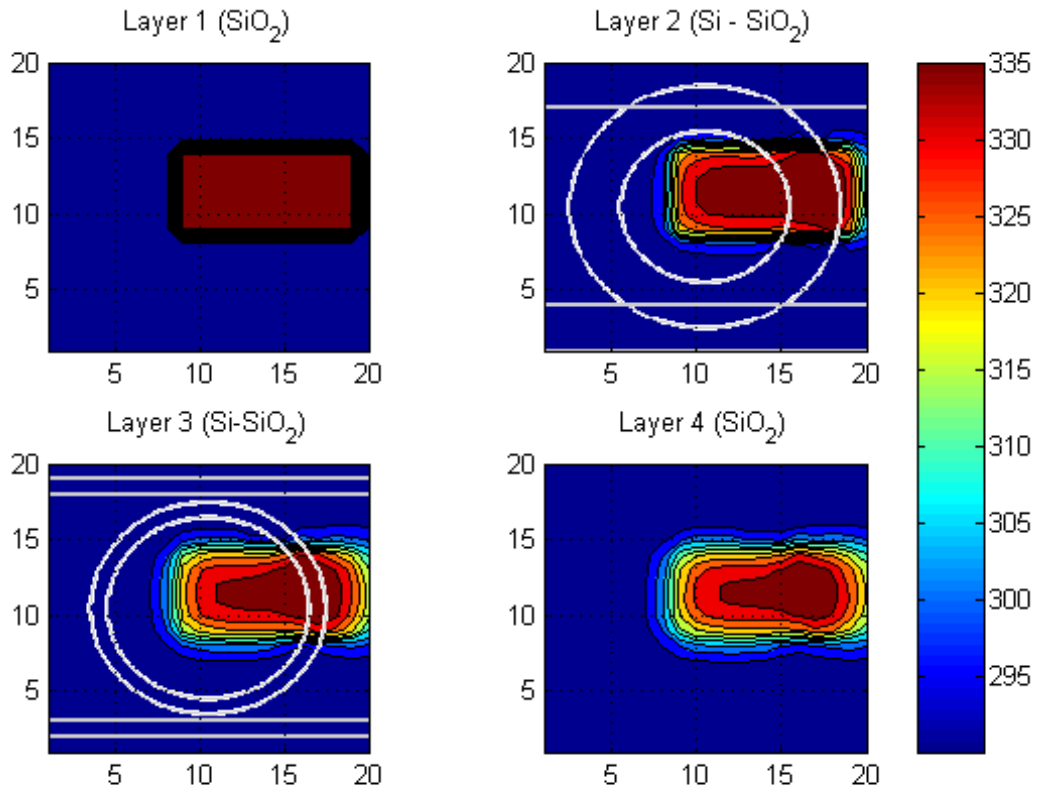


Figure 4.9: 3D FDM - ring resonator example

conditions above and below on the z-axis. The outlined structure of Layer 2 is larger than that of Layer 3 because of the inherent nature of the ridge waveguide's structure (Fig. 4.3). In this case, we see a swing of 45 K. We find in literature that typical temperature swings with $q_{source} = 80 - 100\ W/cm^2$ are equivalent to about 50 K [71]. This shows us that the sources are radiating heat to expected values.

The intended purpose of this thesis is to develop a *thermal characterization abstraction for integrated optoelectronics*. We are interested in this subject due to the cumbersome nature of simulating full-scale simulations and device dependency on temperature. We can do this because temperature is a continuous variable, and intermediate temperatures are found by applying the resistance equations over a domain of cuboid networked resistances. Once the temperatures are known at the interfaces, the coupling problem of heat transfer (Eqn. (3.22)) has effectively has been simplified.

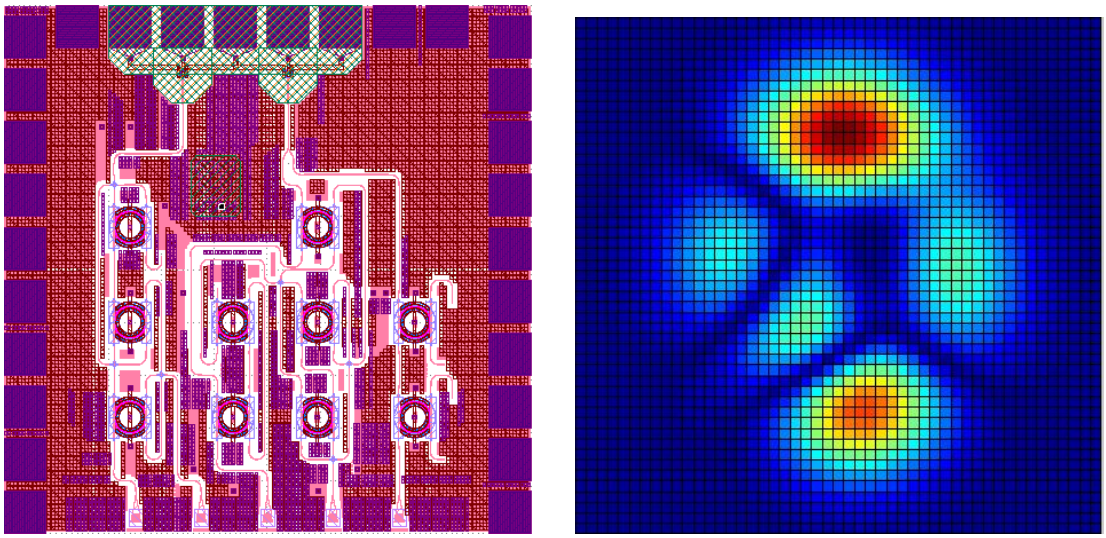
An important aspect of this thesis is to achieve accuracy with minimal discretization.

To validate the accuracy of the model, each experiment should be compared to a full-scale simulation. However, the CAD technology to support such a simulation is not available at this point in time. A design flow to import a GDSII file into a physics modeling software and perform heat conduction studies is as yet unavailable.

4.2 Application to an Optical Layout

Given a photonic layout in GDSII format, as depicted in Fig. 4.10a, and an external thermal gradient, as in Fig. 4.10b with dimensions relative to the layout, we can partition our system into a resistive network. As previously shown in Fig. 4.8, we construct this matrix based on the thermal conductivity composition of each cuboid block. Again, our goal is to estimate the effect of the gradient on *individual devices* within the layout. We need to have a resolution at least an order of magnitude higher than that of the devices themselves to be able to characterize their operation and even more fine for a more accurate representation of the layouts structure. For the rest of the simulations, we will maintain a resolution of the width of a waveguide, $\sim 500\ nm$.

An integrated layout is more complex then the examples demonstrated previously in this section. We only imported the silicon layer into MATLAB and inferred the rest of the area was SiO_2 to keep the examples simple enough to understand the results. A resolution of $\sim 500\ nm$ is accurate to depict all the waveguides in the design. The ring simulated for



(a) Optical four-bit adder design layout

(b) Thermal gradient

Figure 4.10: Optical layout and applied thermal gradient

the three-dimensional example in the previous section is the basic building block of most optical NoC designs – as discussed in a previous section, optical NoCs are the architecture of interest. Although the layout in Fig. 4.10a is not an optical NoC, it closely resembles the structure of one and can be used to represent one for experimental purposes. The structure of an optical NoC consists of row and column oriented ring resonators much like those found in this design.

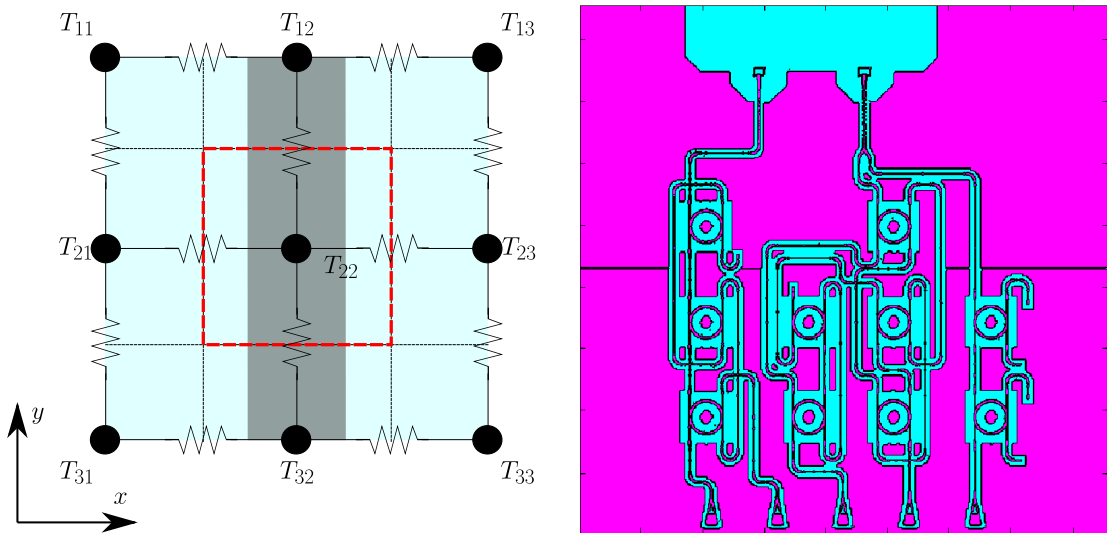
Given that we can determine the ratio of Si to SiO_2 in any square element of our discretization, we can estimate the materials thermal conductivity by weighting the sums based on this ratio. For example, if we assume we have $\sim$ 30% of Si and $\sim$ 60% of SiO_2 in the cuboid element of interest, we can compose k_{eq} as $k_{eq} = 0.3 \cdot k_{Si} + 0.6 \cdot k_{SiO_2}$ where the k's are the thermal conductivities, respectively. While this may not be an accurate continuous representation of the intermediate temperatures within this element, we have discretized our model to only hold accurate in its approximations at the nodes of this discretized representations.

4.2.1 Optical Layout in Two Dimensions

To emphasize the characteristic differences in implementation in two- and three- dimensions, we will first simulate heat flow using the two-dimensional modeling scheme. Using an optical layout consisting of ring resonators and waveguides (Fig. 4.10a), we first read the GDSII file and remove all layers except the Si and SiO_2 layers. We then construct our matrix of conductivity values corresponding to material composition as shown in Fig. 4.11b.

If we assume the block (outlined in Fig. 4.11a) as roughly $\sim$ 50 % Si and $\sim$ 50 % SiO_2, then we can construct our conductivity value for the region as $0.5 \cdot k_{Si} + 0.5 \cdot k_{SiO_2}$. Furthermore, when composing the conductivity $k_{thermal}$ from point $ij \rightarrow kl$, we will compute the conductivity, again, as a percentage. However, this percentage will always be computed using a 50/50 composition for this experiment – the distance to any neighbor node will be the same, resulting in $\Delta L/2$ traversal of each block where ΔL is the distance between any two neighboring nodes.

Employing this matrix generation methodology on the layout in Fig. 4.10a, we extract an approximation – the result is depicted in Fig. 4.11b. The darker area represents the



(a) Conductivity region

(b) Conductivity representation of layout

Figure 4.11: Conductivity examples

higher conductivity, Si, and the lighter area represents the lower conductivity, SiO_2.

Simulating the layout using the FDM method described in the previous chapter and the ADI algorithm, we reach the results depicted in Fig. 4.12. The only difference between this simulation and the single ring simulation in Sec. 4.1.2 is that the resolution is higher here ($\sim$ 2 orders of magnitude) to be able to represent the small sized waveguides in the layout. Using the gradient in Fig. 4.10b, the simulation is performed for the optical layout. The results depicted in Fig. 4.12 show how heat conducts using a 2D model approximation. As we can see, there is an $\sim 9\ K$ swing in temperature. As noted in literature, this maximum source value should produce $\sim 50\ K$ swing in temperature. As the results of the previous experiments in two dimensions, we can conclude that the 2D simulation is lacking valuable information to produce normal results.

4.2.2 Optical Layout in Three Dimensions

Three-dimensional analysis depicts the most accurate representation of the actual behavior of the layouts because they are 3D and have boundary conditions on all sides. In the two-dimensional case, accurate representations cannot be achieved because the information about heat sinks and free convection below cannot be modeled. With the added dimensions, we will be able to see how heat flows through and/or around the different materials. We follow the same methodology as before, but now we have an added

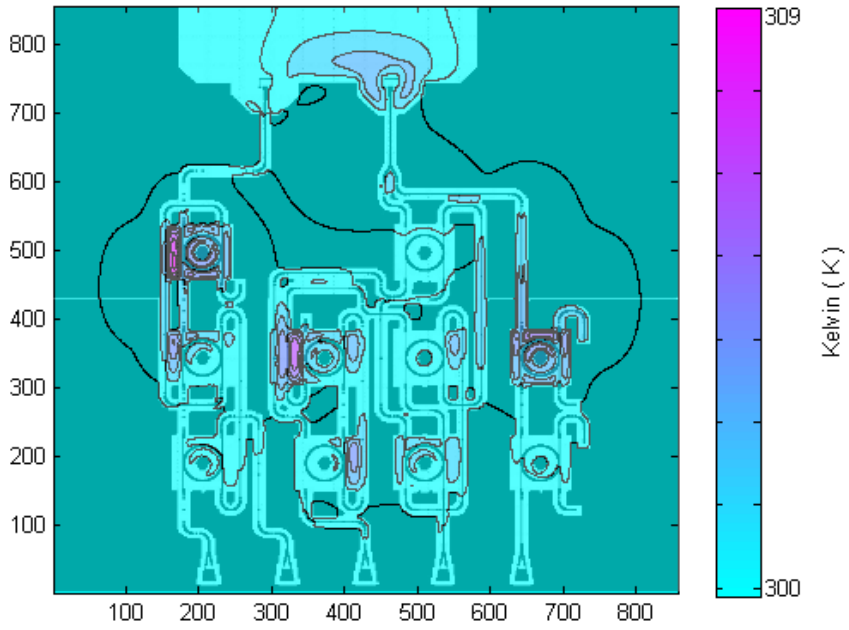


Figure 4.12: 2D-FDM heat conductance on optical layout

dimension. The matrix is generated on a layer-by-layer basis as depicted in Fig. 4.13.

We choose the layers such that they accurately represent the changing dimensions in the z-direction. Due to the planar geometries found in contemporary CMOS manufacturing, we are able to do this easily. We imported the layers one-by-one to generate a two-dimensional representation in matrix form for each layer and connect them together by resistors – a node (ij) of one layer connects to the corresponding node (ij) on the next layer.

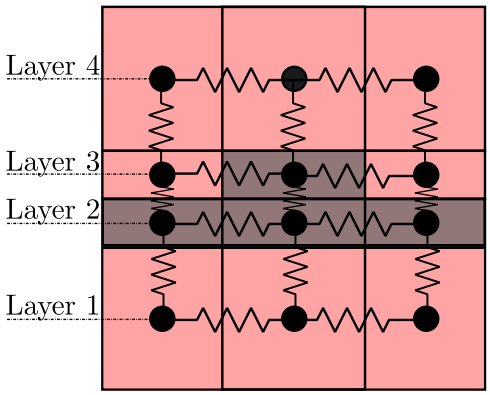


Figure 4.13: Networking over the third spatial dimension

Importing this layout into a 3D model proved to be challenging due to the limitations of reading GDSII layouts into MATLAB without a technology file. Because not enough information is contained in only the GDSII file, the dimensions of each layer are assumed. Fig. 4.14 shows the contour map of the thermal conductivity of each layer in the 3D simulation. The top and bottom layer are just constant because there are no other materials other than SiO_2.

The results of the 3D simulation for the layout are shown in Fig. 4.15. Again, we see that silicon is taking the bulk of the flux due to its higher thermal conductivity. But as we can see from the results, there is definitely an effect on some of the devices.

From the results shown in this chapter, we can see that heat does penetrate through the layers of the layout and stress individual devices. From the data gathered here, we can see that these devices need to be handled with special constraints while designing. Otherwise, we may find that the impacted ring resonators will not function as anticipated or they will consume more power than expected through constant active compensation. With this

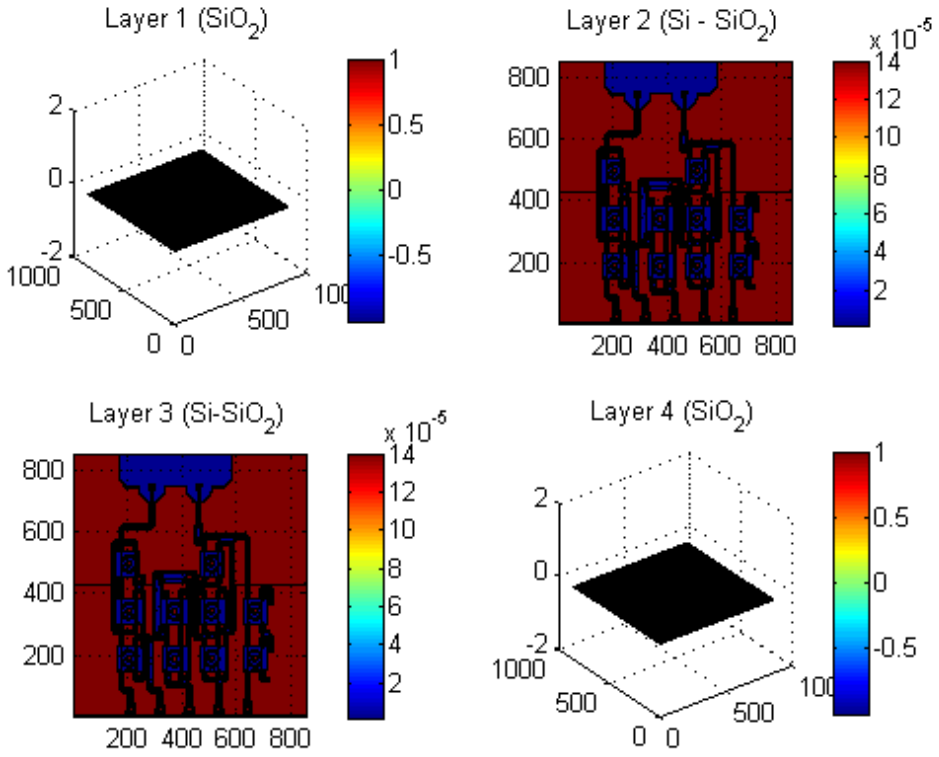


Figure 4.14: 3D-thermal conductivity model

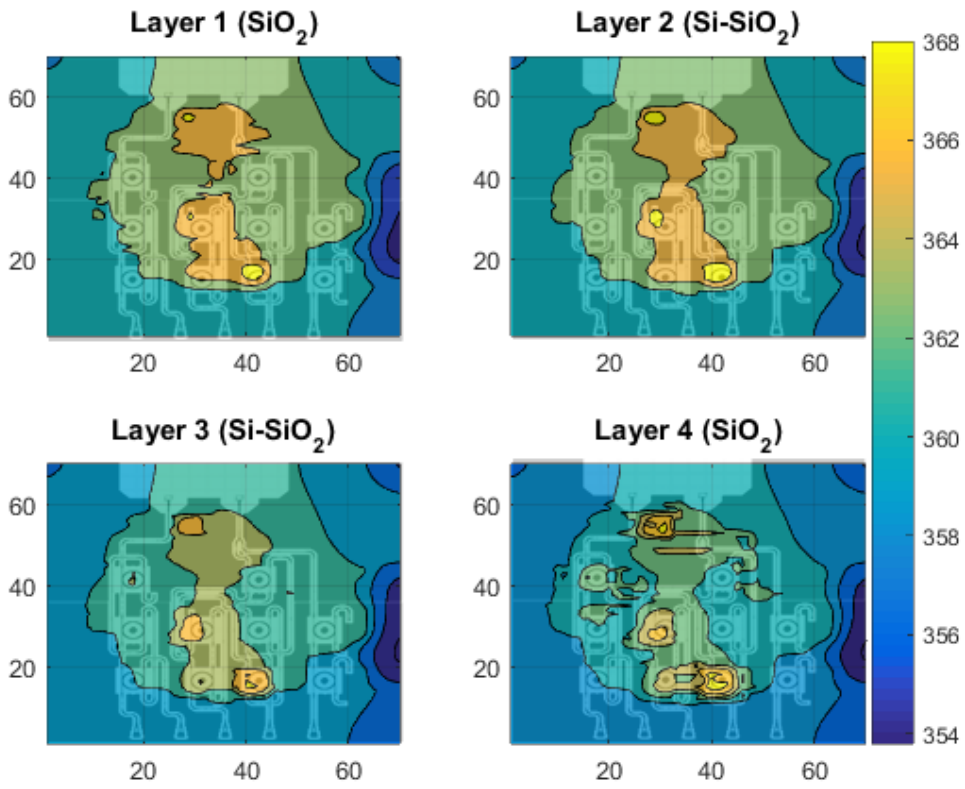


Figure 4.15: 3D-FDM heat conductance on optical layout

information in mind, what can be done about these devices? We will explore that idea in more detail in the next chapter.

As noted in the results section, we have no way to confirm our results due to the lack of tools to perform this coupled computation. Physics-based modeling software packages cannot not successfully import a GDSII file format with optical devices. Current technology will not render the optical design structures correctly because they are not standard CMOS shapes.

CHAPTER 5

APPLICATION TO THERMAL AWARE DESIGN

Chapter 3 shows that a thermal gradient influences the index of refraction, resulting in modulation (Eqn. (3.14)). The resistive equivalence networks solved in Chapter 4 can be directly translated into a refractive index change (Eqn. (3.26)). Applied to the optical design flow, the problem has been reduced into a less complex computation. With this information, we can influence the design flow through passive compensation techniques. This was our objective; we wanted a method of finding temperature throughout the layout for the purpose of compensation to mitigate the degree of thermal stress.

5.1 Compensation for Ring Resonators

Consider the reference ring resonator structure depicted in Fig. 5.1. This ring resonator is a 4-port structure, enabling the ring to demultiplex light entering from the *input-port* to the *drop-port* at the same resonant wavelength(s) as the 2-port ring; nonresonant wavelengths pass to the *through-port*. We define $n_{eff,0}$ as the effective index of the waveguide in the *absence* of a thermal variation, i.e. $T = T_0$. A change in temperature ΔT results in a change to the effective index due to the thermo-optic properties of the waveguide materials, notably in the waveguide's silicon guiding layer. This change in refractive index, in turn, causes a change to the waveguide's propagation constant. Let $n_{eff,0}$ and $\beta_{\Delta T}$, respectively, denote the effective index and propagation constant in the presence of a temperature change $T = T_0 + \Delta T$:

$$n_{eff,0}\Big|_{\Delta T} = n_{eff,\Delta T} \qquad\qquad \beta_0\Big|_{\Delta T} = \beta_{\Delta T} \tag{5.1}$$

The change in propagation constant causes the ring to shift out of resonance as governed by the *resonance condition* in Eqn. (3.20). This shift can be compensated in multiple ways: 1) active compensation using external effects, such as heat, electric fields, etc., 2)

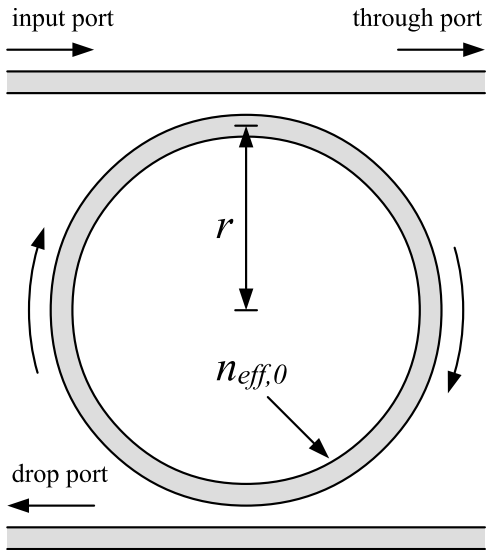


Figure 5.1: Original uncompensated ring

material-level compensation, and 3) geometric changes to device or waveguide structure.

5.1.1 Active Compensation

Active compensation (tuning) utilizes external effects to change the optical properties of materials. For SOI ring resonators, active tuning is usually implemented via micro-heaters [73] — exploiting silicon's relatively large thermo-optic coefficient of $1.86 \times 10^4 / K$. Tuning can also be performed by using carrier injection, by applying a DC-bias to the ring [74]. In all such active compensation methods, outside energy and feedback are required to prevent resonance wavelength drift and offset.

Channel-remapping approaches [75] have been proposed as a means to reduce active power. These approaches reassign WDM channels to different rings depending on their perturbed resonance conditions and require active tuning power. The drawback to this approach is that a larger number of rings are necessary to enable channel remapping, and rings may conflict should their filtering response be similar.

5.1.2 Material-level Passive Compensation

Permanent compensation can be achieved by manipulating the optical properties of a waveguide's materials — i.e. "trimming." Trimming is often performed by affecting the waveguide's cladding layer through stress or additional material layers [76, 77], or by introducing materials that counteract the thermo-optic coefficient of silicon, such as

polymers on narrowed waveguides [78]. Such methods require additional materials and lithographic processes that increase the cost and complexity of fabrication. In addition, materials such as polymers on narrowed waveguides can affect mode confinement, disallowing sharp bends [62].

5.2 Geometric Compensation

Our emphasis is on manipulations to the geometry of the device or waveguide structure — *geometric compensation*. This is an attractive option because modifications to devices can be performed without special process steps, materials, or relying on active compensation. For ring resonators, this involves changes to parameters such as the ring length, or the profile-dimensions of the ring's waveguide. Geometric compensation can be handled through a change in radius (Δr) or through a change in the length (ΔL) of a racetrack resonator.

5.2.1 Compensation Using Ring Radius (r_{comp})

The first compensation method involves changing the radius of the ring (r). This is accomplished by changing the parameter (r_{comp}) in Fig. 5.2. Changes to r_{comp} are inversely proportionate to the temperature-induced change to n_{eff}. Rearranging Eqn. (3.20) for a

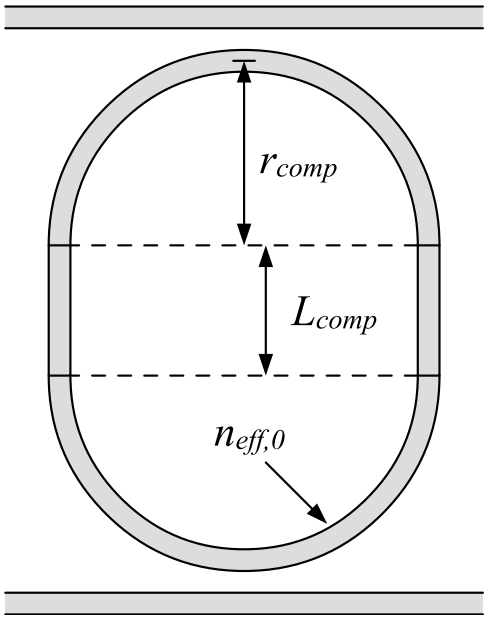


Figure 5.2: Racetrack (ring) resonator

temperature change and replacing L with $2\pi r$ (the length around a circle) results in:

$$\Delta r = \frac{m\lambda}{2\pi}\left(\frac{1}{n_{eff,\Delta T}} - \frac{1}{n_{eff,0}}\right) \tag{5.2}$$

We would like a value of Δr that can be fabricated by existing semiconductor processes (e.g. 22 μm) with a reasonable level of resolution. This implies a 2x factor in resolution — $\Delta r = 44\ \mu m$ at 22 μm — to achieve a reasonable level of accuracy. In silicon photonic processes, temperature-induced variations to n_{eff} are on order of the thermo-optic coefficient of the guiding layer, in this case that of silicon ($\approx 1.84 \times 10^{-4}/K$). When evaluating Eqn. (5.2), this represents a very small differential quantity. For example, with an $n_{eff,0} = 2.6250$ and $\Delta T = 10\ K$ at $\lambda = 1550\ \mu m$, we have:

$$\Delta r = \frac{m \cdot 1550\ \mu m}{2\pi} \cdot \left(\frac{1}{2.650 + 10\ K \cdot 1.84 \times 10^{-4}/\ K} - \frac{1}{2.6250}\right) \tag{5.3}$$

$$= \frac{m \cdot 1550\ \mu m}{2\pi} \cdot (-2.668 \times 10^{-4}) \tag{5.4}$$

$$= m \cdot (-65.8\ nm) \tag{5.5}$$

This implies a change in radius (r) required to compensate this ring is $\sim 65.8\ nm$. To achieve a resolution on order of 44 μm, we must have $m \approx 700$, implying a total ring length $700 \cdot 1550\ \mu m/2.6250 \approx 413\ \mu m$. Though area is always a concern, a ring this size is not especially large and can be easily fabricated. More important, however, the length of the ring affects the ring's spectral characteristics, notably its FSR. A ring of length 413 μm has an FSR on order of:

$$\text{FSR} = \Delta\lambda = \frac{\lambda^2}{n_g L} \tag{5.6}$$

$$= \frac{(1550\ \mu m)^2}{4.63 \cdot 413\ \mu m} \tag{5.7}$$

$$\approx 1.3\ \mu m \tag{5.8}$$

where $n_g = 4.63$ is the precalculated group index for the silicon waveguide profile in this example[1]. An FSR of 1.3 μm is exceptionally small for many applications such as WDM, which require greater spacing between drop wavelengths. Therefore, using only radial length compensation is not a feasible option, but a combination of length or a racetrack and change in radial length is another option.

[1] An SOI rib waveguide of dimensions $w = 400\ \mu m$ and $h = 180\ \mu m$

5.2.2 Compensation Using Racetrack Length (L_{comp})

Consider the racetrack (ring) resonator depicted in Fig. 5.2. The racetrack structure is designed to be equivalent to that of Fig. 5.1 in terms of its resonant wavelength λ and total ring length L. The structure, however, incorporates two compensation regions of length L_{comp} such that $L = 2\left(\pi r_{comp} + L_{comp}\right)$ satisfies Eqn. (3.20). By varying the parameter L_{comp}, facilitating a ring-length change, we can compensate for changes in refractive index.

Incorporating the above L into Eqn. (3.27) we have

$$m\lambda_0 = 2\left(\pi r_{comp} + L_{comp}\right)\left(n_{eff,0} + \frac{dn}{dT}\Delta T\right) \tag{5.9}$$

where dn/dT is the thermo-optic coefficient of the waveguide structure, which is on the order of that of the guiding silicon layer ($\frac{dn}{dT} \approxeq 1.86 \times 10^{-4}/K$). Rearranging for L_{comp} gives us:

$$L_{comp} = \frac{m\lambda_0}{2\left(n_{eff,0} + \frac{dn}{dT}\Delta T\right)} - \pi r_{comp} \tag{5.10}$$

From Eqn. (5.10) we wish to determine the change in L_{comp} as a function of temperature change. This leads to the expression:

$$\Delta L_{comp} = \frac{m\lambda_0}{2\left(n_{eff,0} + \frac{dn}{dT}\Delta T\right)} - \pi r_{comp} - \left(\frac{m\lambda_0}{2n_{eff,0}} - \pi r_{comp}\right) \tag{5.11}$$

$$= \frac{m\lambda_0}{2}\left(\frac{1}{n_{eff,0} + \frac{dn}{dT}\Delta T} - \frac{1}{n_{eff,0}}\right) \tag{5.12}$$

Eqn. (5.12) implies that values of ΔT produce small differential quantities, and likewise small changes to ΔL_{comp}; however, these variations can be multiplied in effect by increasing the ring length through parameter m. For example, consider a ring resonator constructed using a waveguide with dimensions $400\ nm \times 180\ nm$, with $n_{eff,0} = 1.9065$ at the resonant wavelength $\lambda_0 = 1550\ nm$. If this waveguide undergoes a change in temperature $\Delta T = 10\ K$, we have:

$$\Delta L = \frac{m \cdot 1550\ nm}{2} \cdot \left(\frac{1}{1.9065 + 10\ K \cdot 1.86 \times 10^{-4}/K} - \frac{1}{1.9065}\right) \tag{5.13}$$

$$= m \cdot (-0.39620\ nm) \tag{5.14}$$

The effect of the temperature change is therefore so small that ring length must amplify its effects in order for compensation to be effective. If we assume the lithographic process

can fabricate features on the order of $\approx 10\ nm$, the minimum value of m is ≈ 25, implying $L \approx 20.3\ nm$, for compensation at relatively coarse 10 K increments.

Modifying the ring length does have drawbacks. Ensuring precision requires that L must have a minimum length, possibly impacting ring specifications such as FSR, which is inversely proportional to L. Also, in changing the length of the ring, the dimensions of the entire ring structure must be changed. This in turn does not lend itself to a template-based methodology.

CHAPTER 6

CONCLUSION

Integrated optics will be leveraged in hybrid optoelectronic systems, especially for optical communication networks. Electronic switching may create thermal hot-spots that will interact with the optical substrate, producing a thermal gradient. Optical devices such as ring resonators, used in many optical network architectures, are extremely sensitive to temperature-induced changes in refractive index. This causes their resonant wavelength to shift out of spec, affecting their designed operation.

To overcome this problem, we present a *thermal aware characterization abstraction* – an approximation model for estimating temperature at any given placement on an optical layer. We also provide a template for physical resynthesis, using *thermal characterization* data, that exploits perturbation theory applied to waveguide geometry modifications. We provide an automated approach that analyzes simulated data over an uncompensated ring, and derive redesign parameters to enable and achieve passive thermal compensation.

Overall, using this *thermal characterization*, we have demonstrated that optical design can be taken from the behavioral level to the physical level within an automated framework. We present *abstract characterization methods* for modeling heat flow and prepare resynthesis techniques for passive compensation enabling integration into hybrid systems. Our techniques are applied to our own designs and we fabricated a silicon photonic design which is the subject of experiments. Design automation for integrated optics is therefore feasible and a necessary step in the development of the technology and its applications.

6.1 Future Work

This work has addressed one of the many problems to be addressed in design automation for integrated optics. Tremendous opportunities abound in future research in this area, enabling integrated optics to reach its full potential as a communications and computation technology. Areas of future work include: Development of tools for thermal computation

on the fly, Thermal-Aware Placement and Routing, and Prediction of External Gradients.

6.1.1 Tool Development

As integrated optics technology advances, the demand for automation increases. Tool development for on-the-fly thermal computations is an important requirement to the *design automation tool flow – architectural*, *physical*, *circuit*, and *device* design. Most areas of tool development will require the integration of a thermal component. Designing a tool that can read GDSII files directly and convert them to usable models will be necessary. Numerical studies stressed by external gradients can then be performed to provide valuable data on system level integrity.

6.1.2 Thermal-Aware Placement and Routing

While this thesis has demonstrated the use of EDA-style methodologies and made contributions at the thermal characterization level, optical device placement and global routing is a problem that requires a significant amount of further research. More importantly, thermal constraints must be incorporated into the placement and routing models. There has been substantial research in the VLSI domain on thermal-aware placement; however, the integrated optics problem is different. The thermally-aware placement problem for VLSI optimizes a layout to evenly spread out the heat sources as a means to mitigate temperature hot-spots. In integrated optics, however, heat sources are generally external, affecting the optics layers and creating integration challenges. Though we have proposed solutions for thermal compensation of presynthesized devices, the *thermal characterization* proposed here needs to be incorporated into the placement and routing methods models themselves. With such constraints in place, force-directed and other analytical methods would be well suited for such an approach.

6.1.3 External Thermal Gradient Prediction

Thermal-aware placement and compensation approaches also require prediction models for external electrically produced thermal gradients. Though such analysis will depend on circuit activity, the material composition of devices and interconnect regions will play an important role in the thermal model. Drawing inspirations from congestion-based analysis during routing [79], we believe there is great potential to exploit this information

to general thermal maps. These in turn can help guide optical placement when using techniques such as simulated annealing and force-directing.

6.1.4 Uncertainty Quantification Integration

Advances in silicon photonics are enabling hybrid integration of optoelectronic circuits alongside current CMOS technologies. To fully exploit the capability of this integration, it is important to explore the effects of manufacturing uncertainty on optoelectronic devices and systems. The sensitivity of optical components to geometric variation gives rise to design challenges in Silicon On Insulator (SOI) optoelectronic technology. To improve the capability of optical SOI designs, models need to be developed to address the uncertainty quantification problems required to develop reliable systems.

In order to exploit the potential for system-level design optimization, compact models addressing uncertainty quantification problem need to be developed. Uncertainty quantification solvers within the flow of physical design automation tools for hybrid optoelectronic technology could potentially enable device resynthesis and more reliable validation at a system level. A reduced order model eliminating the need for full-scale Monte Carlo or Neural Network simulations in the design process within contemporary CAD flow when designing optoelectronic features will be necessary. Investigation into contemporary models that are used for transistor-level uncertainty quantification is needed and an application using those techniques with variation to the integration of optoelectronic design into today's physical design automation standards would be a next step.

It would be interesting to find out whether uncertainty in silicon photonics is really a liability or could it be treated as an optimization resource in the CAD/synthesis flow. At a high-level/behavior-level (i.e. ignoring low-level implementation challenges), there could be scope to exploit uncertainty in design (e.g. design of physically unclonable functions (PUFs) as security primitives). At this point, it would be hard to determine if this will translate easily at the physical design level but is something to consider.

REFERENCES

[1] L. Liao, D. Samara-Rubio, M. Morse, A. Liu, D. Hodge, D. Rubin, U. D. Keil, T. Franck *et al.*, "High speed silicon mach-zehnder modulator," *Opt. Express*, vol. 13, no. 8, pp. 3129–3135, 2005.

[2] W. M. Green, M. J. Rooks, L. Sekaric, Y. A. Vlasov *et al.*, "Ultra-compact, low rf power, 10 gb/s silicon mach-zehnder modulator," *Optics Express*, vol. 15, no. 25, pp. 17 106–17 113, 2007.

[3] H. Rong, R. Jones, A. Liu, O. Cohen, D. Hak, A. Fang, and M. Paniccia, "A continuous-wave raman silicon laser," *Nature*, vol. 433, no. 7027, pp. 725–728, 2005.

[4] H. Park, A. W. Fang, S. Kodama, and J. E. Bowers, "Hybrid silicon evanescent laser fabricated with a silicon waveguide and iii-v offset quantum wells," *Optics Express*, vol. 13, no. 23, pp. 9460–9464, 2005.

[5] M. J. Heck, H.-W. Chen, A. W. Fang, B. R. Koch, D. Liang, H. Park, M. N. Sysak, and J. E. Bowers, "Hybrid silicon photonics for optical interconnects," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 17, no. 2, pp. 333–346, 2011.

[6] B. Analui, D. Guckenberger, D. Kucharski, and A. Narasimha, "A fully integrated 20-gb/s optoelectronic transceiver implemented in a standard 0.13-¡ formula formulatype=," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 12, pp. 2945–2955, 2006.

[7] O. Boyraz, P. Koonath, V. Raghunathan, B. Jalali *et al.*, "All optical switching and continuum generation in silicon waveguides," *Optics Express*, vol. 12, no. 17, pp. 4094–4102, 2004.

[8] M. J. Cianchetti, J. C. Kerekes, and D. H. Albonesi, "Phastlane: a rapid transit optical routing network," in *ACM SIGARCH Computer Architecture News*, vol. 37, no. 3. ACM, 2009, pp. 441–450.

[9] R. Beausoleil, J. Ahn, N. Binkert, A. Davis, D. Fattal, M. Fiorentino, N. Jouppi, M. McLaren, C. Santori, R. Schreiber *et al.*, "A nanophotonic interconnect for high-performance many-core computation," in *High Performance Interconnects, 2008. HOTI'08. 16th IEEE Symposium on*. IEEE, 2008, pp. 182–189.

[10] J. Chan, G. Hendry, K. Bergman, and L. P. Carloni, "Physical-layer modeling and system-level design of chip-scale photonic interconnection networks," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 30, no. 10, pp. 1507–1520, 2011.

[11] S. J. Emelett and R. Soref, "Design and simulation of silicon microring optical routing switches," *Journal of Lightwave Technology*, vol. 23, no. 4, p. 1800, 2005.

[12] C. Condrat, P. Kalla, and S. Blair, "Logic synthesis for integrated optics," in *Proceedings of the 21st Edition of the Great Lakes Symposium on VLSI*. ACM, 2011, pp. 13–18.

[13] H. J. Caulfield, C. S. Vikram, and A. Zavalin, "Optical logic redux," *Optik-International Journal for Light and Electron Optics*, vol. 117, no. 5, pp. 199–209, 2006.

[14] A. Politi, J. C. Matthews, and J. L. O'Brien, "Shors quantum factoring algorithm on a photonic chip," *Science*, vol. 325, no. 5945, pp. 1221–1221, 2009.

[15] A. Poustie and K. Blow, "Demonstration of an all-optical fredkin gate," *Optics Communications*, vol. 174, no. 1, pp. 317–320, 2000.

[16] S. Kotiyal, H. Thapliyal, and N. Ranganathan, "Mach-zehnder interferometer based design of all optical reversible binary adder," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2012*. IEEE, 2012, pp. 721–726.

[17] A. Qouneh, Z. Li, M. Joshi, W. Zhang, X. Fu, and T. Li, "Aurora: A thermally resilient photonic network-on-chip architecture," in *Computer Design (ICCD), 2012 IEEE 30th International Conference on*. IEEE, 2012, pp. 379–386.

[18] C. K. Madsen and J. H. Zhao, *Optical filter design and analysis: a signal processing approach*. Wiley, 2001.

[19] "IBM Research: Silicon Integrated Nanophotonics," http:// www.research.ibm.com/ photonics.

[20] "Nanophotonics and Quantum Optics," http:// www.hpl.hp.com/ research/ qsr/ quantumoptics.html.

[21] "OpSIS: Optoelectronic System Integration in Silicon," http:// depts.washington.edu/ uwopsis.

[22] D. Ding and D. Z. Pan, "Oil: a nano-photonics optical interconnect library for a new photonic networks-on-chip architecture," in *Proceedings of the 11th International Workshop on System Level Interconnect Prediction*. ACM, 2009, pp. 11–18.

[23] D. Ding, Y. Zhang, H. Huang, R. T. Chen, and D. Z. Pan, "O-router: an optical routing framework for low power on-chip silicon nano-photonic integration," in *Proceedings of the 46th Annual Design Automation Conference*. ACM, 2009, pp. 264–269.

[24] J. S. Orcutt and R. J. Ram, "Photonic device layout within the foundry cmos design environment," *Photonics Technology Letters, IEEE*, vol. 22, no. 8, pp. 544–546, 2010.

[25] D. Ding, B. Yu, and D. Z. Pan, "Glow: A global router for low-power thermal-reliable interconnect synthesis using photonic wavelength multiplexing," in *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific*. IEEE, 2012, pp. 621–626.

[26] C. Condrat, P. Kalla, and S. Blair, "Exploring design and synthesis for optical digital logic," in *International Workshop on Logic Synthesis*, 2010.

[27] ——, "A methodology for physical design automation for integrated optics," in *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2012, pp. 598–601.

[28] ——, "Channel routing for integrated optics," in *System Level Interconnect Prediction (SLIP), 2013 ACM/IEEE International Workshop on*. IEEE, 2013, pp. 1–8.

[29] ——, "Crossing-aware channel routing for photonic waveguides," in *Proceedings of IEEE International Midwest Symposium on Circuits and Systems*, 2013.

[30] J.-L. Tsai, C.-P. Chen, G. Chen, B. Goplen, H. Qian, Y. Zhan, S.-M. Kang, M. D. Wong, and S. S. Sapatnekar, "Temperature-aware placement for socs," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1502–1518, 2006.

[31] Y. Vlasov, "Silicon photonics for next generation computing systems," in *European Conference on Optical Communications*, 2008.

[32] T. Zhang, Y. Zhan, and S. S. Sapatnekar, "Temperature-aware routing in 3d ics," in *Design Automation, 2006. Asia and South Pacific Conference on*. IEEE, 2006, pp. 6–pp.

[33] B. Goplen and S. Sapatnekar, "Efficient thermal placement of standard cells in 3d ics using a force directed approach," in *Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design*. IEEE Computer Society, 2003, p. 86.

[34] J. Hudgings, K. Pipe, and R. Ram, "Thermal profiling for optical characterization of waveguide devices," *Applied Physics Letters*, vol. 83, no. 19, pp. 3882–3884, 2003.

[35] M. Huang and X. Yan, "Thermal-stress effects on the temperature sensitivity of optical waveguides," *JOSA B*, vol. 20, no. 6, pp. 1326–1333, 2003.

[36] J. Hardy and J. Shamir, "Optics inspired logic architecture," *Optics Express*, vol. 15, no. 1, pp. 150–165, 2007.

[37] H. John Caulfield, R. A. Soref, L. Qian, A. Zavalin, and J. Hardy, "Generalized optical logic elements–goles," *Optics Communications*, vol. 271, no. 2, pp. 365–376, 2007.

[38] *RSoft Photonics CAD Suite*, RSoft Inc., www.rsoftdesign.com.

[39] *Lumerical Photonic Design Software*, Lumerical Computational Solutions, Inc., www.lumerical.com.

[40] L. Thylén and L. Wosinski, "Integrated photonics in the 21st century," *Photonics Research*, vol. 2, no. 2, pp. 75–81, 2014.

[41] S. E. Miller, "Integrated optics: An introduction," *Bell System Technical Journal*, vol. 48, no. 7, pp. 2059–2069, 1969.

[42] M. Stolarska and D. Chopp, "Modeling thermal fatigue cracking in integrated circuits by level sets and the extended finite element method," *International Journal of Engineering Science*, vol. 41, no. 20, pp. 2381–2410, 2003.

[43] M. Streshinsky, R. Ding, Y. Liu, A. Novack, C. Galland, A.-J. Lim, P. Guo-Qiang Lo, T. Baehr-Jones, and M. Hochberg, "The road to affordable, large-scale silicon photonics," *Optics and Photonics News*, vol. 24, no. 9, pp. 32–39, 2013.

[44] C. K. Madsen and J. H. Zhao, *Optical filter design and analysis*. Wiley-Interscience, 1999.

[45] D. A. Miller, "Optical interconnects to electronic chips," *Applied Optics*, vol. 49, no. 25, pp. F59–F70, 2010.

[46] K. Preston, B. Schmidt, and M. Lipson, "Polysilicon photonic resonators for large-scale 3d integration of optical networks," *Optics Express*, vol. 15, no. 25, pp. 17 283–17 290, 2007.

[47] C. A. Brackett, A. S. Acampora, J. Sweitzer, G. Tangonan, M. T. Smith, W. Lennon, K.-C. Wang, and R. H. Hobbs, "A scalable multiwavelength multihop optical network: A proposal for research on all-optical networks," *Lightwave Technology, Journal of*, vol. 11, no. 5, pp. 736–753, 1993.

[48] A. Joshi, C. Batten, Y.-J. Kwon, S. Beamer, I. Shamim, K. Asanovic, and V. Stojanovic, "Silicon-photonic clos networks for global on-chip communication," in *Proceedings of the 2009 3rd ACM/IEEE International Symposium on Networks-on-Chip*. IEEE Computer Society, 2009, pp. 124–133.

[49] Y. Ye, L. Duan, J. Xu, J. Ouyang, M. K. Hung, and Y. Xie, "3d optical networks-on-chip (noc) for multiprocessor systems-on-chip (mpsoc)," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*. IEEE, 2009, pp. 1–6.

[50] K. Bergman, L. P. Carloni, A. Biberman, J. Chan, and G. Hendry, "Photonic network architectures i: Circuit switching," in *Photonic Network-on-Chip Design*. Springer, 2014, pp. 101–164.

[51] S. Rzepka, K. Banerjee, E. Meusel, and C. Hu, "Characterization of self-heating in advanced vlsi interconnect lines based on thermal finite element simulation," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 21, no. 3, pp. 406–411, 1998.

[52] H.-Y. Ng, M. R. Wang, D. Li, X. Wang, J. Martinez, R. R. Panepucci, and K. Pathak, "4$\times$ 4 wavelength-reconfigurable photonic switch based on thermally tuned silicon microring resonators," *Optical Engineering*, vol. 47, no. 4, pp. 044 601–044 601, 2008.

[53] B. Guha, B. B. Kyotoku, and M. Lipson, "Cmos compatible athermal silicon microring resonators," *arXiv*, 2009.

[54] C. Pollock and M. Lipson, *Integrated photonics*. Springer, 2003.

[55] J. Gao, *Optoelectronic integrated circuit design and device modeling*. Wiley, 2011.

[56] Y. Zhan and S. S. Sapatnekar, "Fast computation of the temperature distribution in vlsi chips using the discrete cosine transform and table look-up," in *Proceedings of the 2005 Asia and South Pacific Design Automation Conference*. ACM, 2005, pp. 87–92.

[57] ——, "A high efficiency full-chip thermal simulation algorithm," in *Proceedings of the 2005 IEEE/ACM International Conference on Computer-Aided Design*. IEEE Computer Society, 2005, pp. 635–638.

[58] J. Lee, "Thermal placement algorithm based on heat conduction analogy," *Components and Packaging Technologies, IEEE Transactions on*, vol. 26, no. 2, pp. 473–482, 2003.

[59] B. Goplen and S. Sapatnekar, "Thermal via placement in 3d ics," in *Proceedings of the 2005 International Symposium on Physical Design*. ACM, 2005, pp. 167–174.

[60] A. Boos, L. Ramini, U. Schlichtmann, and D. Bertozzi, "Proton: an automatic place-and-route tool for optical networks-on-chip," in *Computer-Aided Design (ICCAD), 2013 IEEE/ACM International Conference on*. IEEE, 2013, pp. 138–145.

[61] E. S. Bahaa and C. T. Malvin, *Fundamentals of photonics*, 2nd ed. New York/A WILEY-INTERSCIENCE PUBLICATION, 2007.

[62] W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, "Silicon microring resonators," *Laser & Photonics Reviews*, vol. 6, no. 1, pp. 47–73, 2012.

[63] V. Passaro and F. De Leonardis, "Recent advances in modelling and simulation of silicon photonic devices," *Modelling and Simulation*, pp. 367–90, 2008.

[64] S. Manipatruni, R. K. Dokania, B. Schmidt, N. Sherwood-Droz, C. B. Poitras, A. B. Apsel, and M. Lipson, "Wide temperature range operation of micrometer-scale silicon electro-optic modulators," *Optics Letters*, vol. 33, no. 19, pp. 2185–2187, 2008.

[65] R. L. Burden and J. D. Faires, *Numerical analysis*, 9th ed. Brooks/Cole, 2011.

[66] J. Holman, *Heat transfer*, 10th ed. McGraw-Hill, New York, 2010.

[67] D. D. Mooney and R. J. Swift, *A course in mathematical modeling*. Cambridge University Press, 1999.

[68] J. H. Lienhard, *A heat transfer textbook*. Courier Dover Publications, 2011.

[69] Wikipedia. (2014) Silicon — wikipedia, the free encyclopedia. [Accessed 30-April-2014]. [Online]. Available: http://http://en.wikipedia.org/wiki/Silicon

[70] ——. (2014) Silicon dioxide — wikipedia, the free encyclopedia. [Accessed 30-April-2014]. [Online]. Available: http://http://en.wikipedia.org/wiki/Silicon_dioxide

[71] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Research*, vol. 3, no. 3, pp. 147–169, 2010.

[72] A. Tech. (2014, Apr.) Estimating heat transfer coefficients. [Online]. Available: http://altasimtechnologies.com/ electronic-cooling/ estimating-heat-transfer-coefficients/

[73] F. Gan, T. Barwicz, M. Popovic, M. Dahlem, C. Holzwarth, P. Rakich, H. Smith, E. Ippen, and F. Kartner, "Maximizing the thermo-optic tuning range of silicon photonic structures," in *Photonics in Switching*, 2007, pp. 67–68.

[74] C. Shih, Z. W. Zeng, and S. Chao, "Extinction ratio compensation by free carrier injection for a mos-capacitor microring optical odulator subjected to temperature drifting," in *Conference on Lasers and Electro-Optics/Pacific Rim*. Optical Society of America, 2009, p. TUP27.

[75] Y. Zheng, P. Lisherness, M. Gao, J. Bovington, K.-T. Cheng, H. Wang, and S. Yang, "Power-efficient calibration and reconfiguration for optical network-on-chip," *Journal of Optical Communications and Networking*, vol. 4, no. 12, pp. 955–966, 2012.

[76] J. Schrauwen, D. Van Thourhout, and R. Baets, "Trimming of silicon ring resonator by electron beam induced compaction and strain," *Optics Express*, vol. 16, no. 6, pp. 3738–3743, 2008.

[77] S. Lambert, W. De Cort, J. Beeckman, K. Neyts, and R. Baets, "Trimming of silicon-on-insulator ring resonators with a polymerizable liquid crystal cladding," *Optics Letters*, vol. 37, no. 9, pp. 1475–1477, 2012.

[78] J. Teng, P. Dumon, W. Bogaerts, H. Zhang, X. Jian, M. Zhao, G. Morthier, and R. Baets, "Athermal soi ring resonators by overlaying a polymer cladding on narrowed waveguides," in *6th IEEE International Conference, Group IV Photonics*, 2009, pp. 77–79.

[79] J. Hu, M.-C. Kim, and I. L. Markov, "Taming the complexity of coordinated place and route," in *Design Automation Conference (DAC), 2013 50th ACM/EDAC/IEEE*. IEEE, 2013, pp. 1–7.